

## Quick Guide for Power Losses Calculation in MOSFETS – Part 3

### Approach to Estimate Total MOSFET Power Dissipation

In [Part I](#) of this application note series, equations were developed to estimate MOSFET turn-ON and turn-OFF switching intervals in hard-switching applications. These switching intervals form the basis for estimating switching power dissipation and comparing device performance under dynamic operating conditions.

In [Part II](#), practical methods were introduced to extract key switching parameters from datasheet information, including plateau voltage approximation and equivalent capacitance estimation. These techniques help engineers apply switching loss calculations during early-stage device selection, even when detailed SPICE models are not available.

This third part of the series extends the previous analysis to a more complete MOSFET power loss evaluation. While switching losses are often one of the dominant contributors in high-frequency and high-power-density applications, they are not the only source of dissipation in a practical design. Conduction losses, output capacitance discharge losses, and gate driver losses must also be considered to obtain a realistic estimation of total device power dissipation.

This application note presents practical methods to estimate total MOSFET power losses in a low-side driver circuit with an inductive load. The analysis combines the switching interval calculations introduced in Part I with the datasheet-based parameter extraction methods developed in Part II. A complete calculation example using an MCC Power MOSFET is included and compared with simulation results to demonstrate the accuracy of the approach.

# 1. Introduction

As has been previously stated in past application notes of this series, power losses in MOSFET come from different sources, with switching time losses being one of the most important (see Figure 1a & 1b), especially in higher power density products.

Switching time losses are directly linked to the device's dynamic parameters and hence, the importance of the right MOSFET.

However, a complete picture of Power Losses in a FET should include conduction, output capacitor discharge and gate-driver losses. These topics will be discussed here in detail and, at the end, a complete calculation example of complete Power Losses in a Low-Side Driver with Inductive Load will be presented.

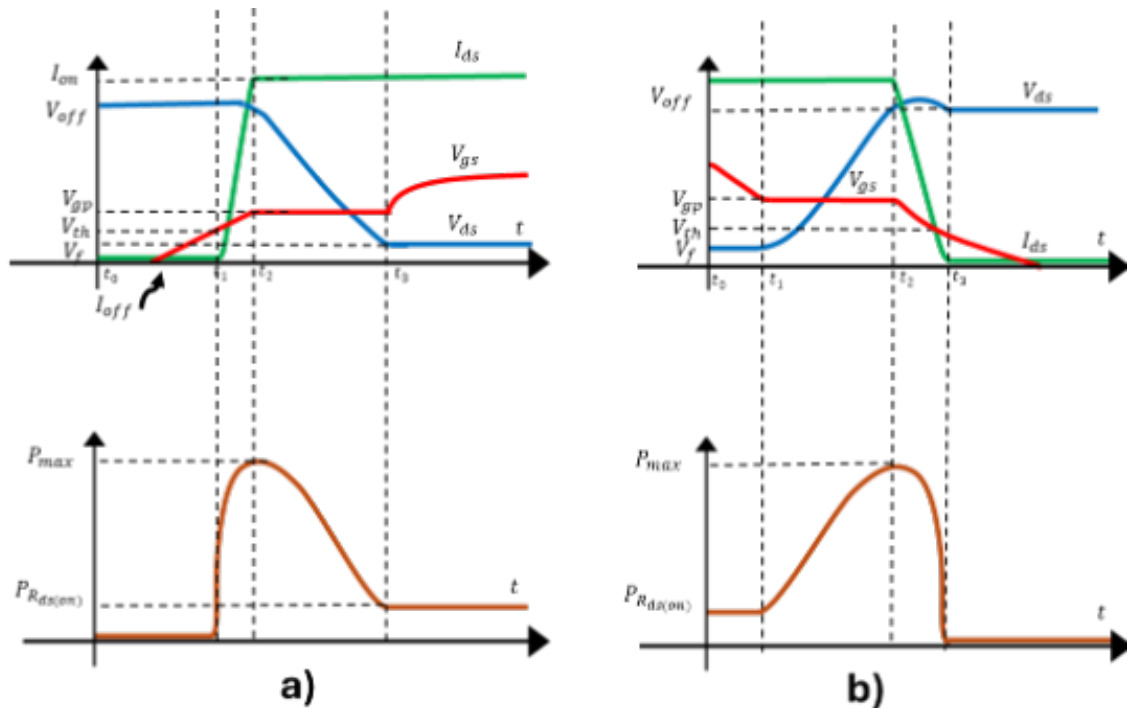


Figure 1. Switching Transition Waveforms for a) ON state and b) OFF state.

## 2. Types of Power Losses on MOSFETs

### 2.1 Switching time losses (ON and OFF)

This type of power loss occurs due to the MOSFET not being an ideal switch, but a practical one, meaning that it will not automatically go from  $v_{DS} = V_{DD}$  while in Off state and to  $v_{DS} = I_0 r_{DS(on)}$  while in ON state. Because of that, as shown in Figure 2 during ON/OFF transitions  $v_{DS} \neq 0$  and  $i_{DS} \neq 0$  occur simultaneously leading to power losses.

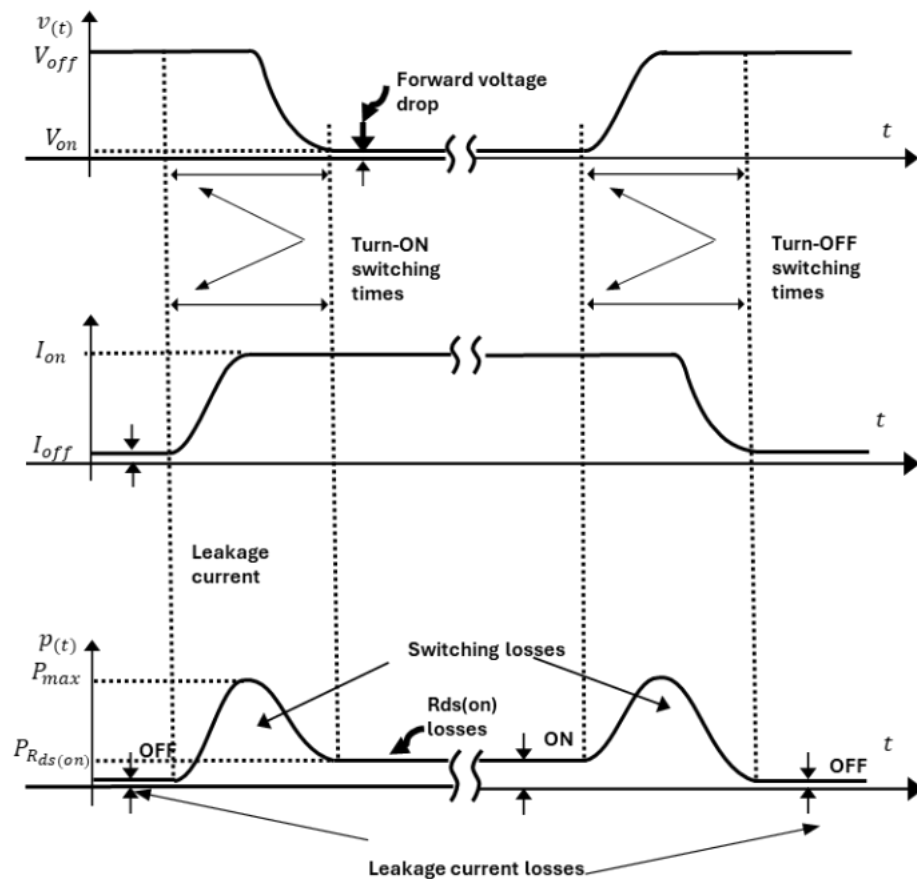


Figure 2. Switching times and power losses.

Using the results from previous Application Notes in this Series [1] the effective switching losses intervals are written as follows:

$$t_{ON} = R_G \cdot C_{iss} \cdot \ln \left( \frac{V_{GG} - V_{th}}{V_{GG} - V_p} \right) + R_G \cdot C_{GD_{Av}} \left( \frac{V_{DD} - I_0 r_{DS(on)}}{V_{GG} - V_p} \right),$$

$$t_{OFF} = R_G \cdot C_{GD_{Av}} \left( \frac{V_{DD} - I_0 r_{DS(on)}}{V_p} \right) + R_G \cdot C_{iss} \cdot \ln \left( \frac{V_p}{V_{th}} \right).$$

We can take  $P_{on}$  and  $P_{off}$  to be the peak power dissipated during ON and OFF transition respectively. Following a simplified and pessimistic triangular waveform shown in Figure 3 (instead of the actual waveform which has a smoother shape) will allow us to calculate the energy values using the area of the triangular waveform:

$$E_{on} = \frac{1}{2} I_0 V_{DD} t_{ON} = \frac{1}{2} P_{on} t_{ON}$$

$$E_{off} = \frac{1}{2} I_0 V_{DD} t_{OFF} = \frac{1}{2} P_{off} t_{OFF}$$

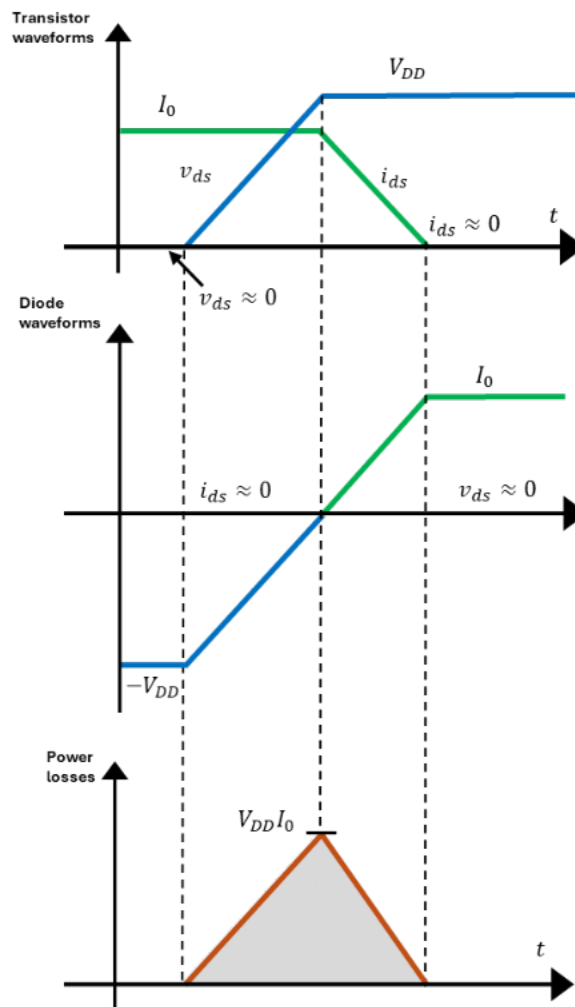


Figure 3. Worst case for switching losses for MOSFET, where the gray area represents energy loss.

These switching losses are described in terms of energy, however, in several references in literature the switching losses are preferably described in terms of average power dissipation. Therefore, we can rewrite the following,

$$P_{sw\_av} = \frac{1}{T} \int_0^T (P_{on} + P_{off}) dt,$$

$$P_{sw\_av} = \frac{1}{T} \left[ \int_0^{t_{ON}} P_{on} dt + \int_0^{t_{OFF}} P_{off} dt \right],$$

but  $f_{sw} = 1/T$ ,

$$P_{sw\_av} = [E_{on} + E_{off}] f_{sw}.$$

## 2.2. Conduction Losses

Figure 1 and Figure 2 show portions of time of the switching period where there are no switching power losses. These time intervals will involve other kinds of losses: conduction losses.

During the time interval before the MOSFET ON transition begins and the MOSFET is completely OFF, the device will draw a very small leakage current, given as Zero Gate Voltage Drain Current ( $I_{DSS}$ ) in datasheets. In this document we will ignore these losses, nevertheless this small current exists.

In the other hand, when the MOSFET is completely ON (after turn-ON transition has completely passed and before turn-OFF transition begins; that is, after  $t_3$  in Figure 1a and before  $t_1$  in Figure 1b),  $v_{DS} = I_0 r_{DS(on)}$  and  $i_{DS} = I_0$ . This time interval is included in the complete Power Losses considering the time where the device remains at the ON-state, thus, the conduction power losses defined by energy are:

$$E_{Cond} = (I_0)^2 r_{DS(on)} DT$$

where  $D$  is the ON duty cycle (fraction of the switching period where the MOSFET is turned ON). This form of power conduction losses is included later in our calculation example. With the average conduction power losses given by:

$$P_{Cond\_av} = (I_0)^2 r_{DS(on)} D.$$

## 2.3 Power losses due to ( $C_{oss}$ )

The output capacitance  $C_{oss}$  does not only affect the switching times or the plateau voltage but is also a source of power losses on its own. This is because the capacitor stores energy while the  $v_{DS}$  is increasing, as seen in Figure 4. The discharge of  $C_{oss}$  only happens while the device is turning ON, hence, the energy must be dissipated in form of power losses every time the MOSFET is activated [1].

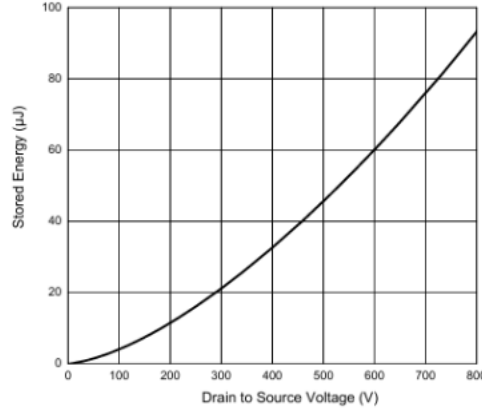


Figure 4. Output capacitor stored charge.

The plot shown in Figure 4 is not always included in MOSFET datasheets, but there are ways to generate this plot from common datasheet information, this explored further in the document. But it is important to note that the energy losses due to  $C_{oss}$  discharge are found with the analysis below, which consist in basic analysis of power in a circuit in energy equations, given by:

$$E = \int_0^t P dt = \int_0^t V I dt,$$

where  $P$  is the power being integrated for a given time  $t$ . But we can define:  $I = dQ/dt$  and  $V = Q/C(v)$  for a capacitor (in this case a non-linear capacitor  $C(v)$ ). Therefore, energy expression is also:

$$E = \int_0^t \frac{Q}{C(v)} \frac{dQ}{dt} dt,$$

$$E = \int_0^Q \frac{Q}{C(v)} dQ.$$

To avoid complex solutions to this equation, the non-linear capacitor can be replaced with an equivalent linear capacitor. Section 3.2 will show how to obtain this equivalent linear capacitor, named here  $C_{oss}$ . Thus, solving the integral above we have:

$$E = \frac{Q^2}{2C} = \frac{C^2 V^2}{2C},$$

$$E_{oss} = \frac{C_{oss}V_{ds}^2}{2}.$$

Then, the average power dissipated due to discharging the MOSFET's Output Capacitor is:

$$P_{oss\_av} = \frac{C_{oss}V_{ds}^2f_{sw}}{2}.$$

## 2.4 Gate driver power losses

For the transistor to turn on and off, it is necessary to have a circuit driver at its gate terminal. Up to this point, we have only analysis transition losses, but the energy to charge and discharge the gate capacitor should come from somewhere. There are plenty of gate driver circuits in several shapes and forms, here it is represented as a Thevenin equivalent in the example circuit used, see Figure 5.

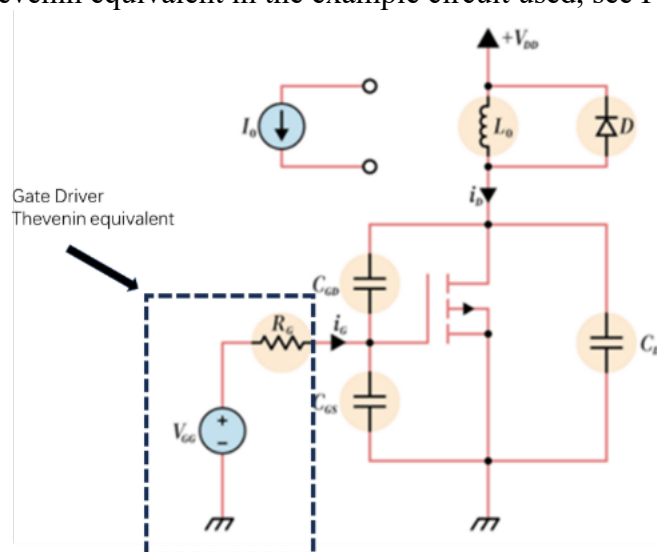


Figure 5. Low side driver circuit with inductive load and Thevenin equivalent at gate terminal.

Following the same analysis done in the previous section with  $C_{oss}$ , we can obtain the energy needed to charge MOSFET input capacitance  $C_{iss}$  as (these losses happen during both transitions and the divided by 2 factor disappears):

$$E_{iss} = C_{iss}V_{GS}^2 = Q_G V_{GS}$$

Where we have used the total gate charge  $Q_G$ , the average power losses due to the gate driver circuit at MOSFET can be calculated as (using  $V_{GG}$  as the gate-to-source voltage):

$$P_{Driver\_av} = Q_G V_{GG} f_{sw}$$

Finally, the total average power losses can be written as:

$$P_{Total\_av} = (P_{sw\_av} + P_{cond} + P_{oss\_av} + P_{Driver\_av}).$$

### 3. Energy Related equivalent output capacitance

As mentioned before in this series,  $C_{iss}$  and  $C_{oss}$  are non-linear capacitances which values strongly depends on  $V_{GG}$  and  $V_{DD}$ . These non-linearities complicate the calculations since  $v_{GD}$  swings from  $V_{DD}$  (off) to  $-V_{GG}$  (on) and  $v_{DS}$  swings from  $V_{DD}$  (off) to  $v_{DS(on)} \approx I_0 r_{DS(on)}$  (on).

For the estimation of the energy related equivalent output capacitance  $C_{oss\_er}$ , the extraction method detailed in Part 2 of this series [2] can be used. The objective is to find an equivalent linear capacitor value with the same energy related to the non-linear capacitor energy at the desired  $V_{DS}$ . To do this, data points in the  $C_{oss}$  capacitance small signal characteristics need to be extracted from the datasheet plot and used to simulate the non-linear charge curve with respect to its terminal voltages using the method in [3] and explained in [4]. This simulation can be used to obtain the plot of the Non-Linear  $C_{oss}$  storage energy with respect to  $V_{DS}$  as shown in Figure 4, and using the following equation, which is derived by the principles stated in [5], and what is seen in Figure 6, where the lined area corresponds to the stored energy:

$$E_{oss}(v) = Q(v) * v - \int Q(v) dv.$$

Given that, using the following capacitor definition, we can obtain an equivalent linear capacitor with the same energy as the non-linear capacitor  $C_{oss}$  at a specific  $V_{DS}$  voltage:

$$C_{oss\_er} = \frac{2E_{oss}(V_{DS})}{V_{DS}^2}.$$

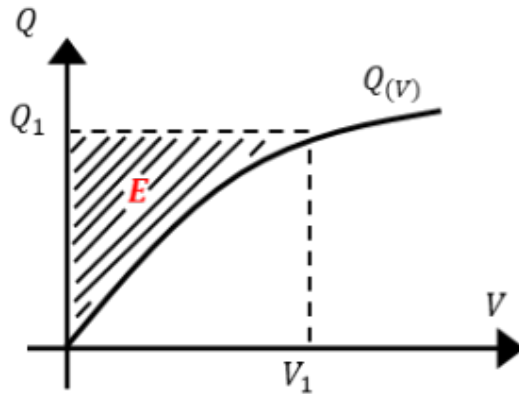


Figure 6. Energy stored in Non-linear capacitor can be found as the shaded area in this plot.

## 4. Power Losses Calculation

As an example, following the procedure previously described above, a calculation for power losses will be done under the analysis of an LSD with an inductive load.

Taking the following values for surrounding conditions on Figure 5 Low-Side driver circuit:  $V_{GG} = 10V$ ,  $V_{DD} = 75V$ ,  $I_o = 15A$ ,  $R_{g_{ext}} = 10\Omega$  an example calculation will be presented here.

For this MCC's Power MOSFET [MCAC15N15Y-TP](#) will be used. Table 1 shows these component parameters that are relevant for this analysis.

Parameter	Symbol	MCAC15N15Y	Conditions
Drain-Source Maximum Voltage	$V_{DS}$	150V	$V_{GS} = 0V, I_D = 250\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	2V to 4V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source On-Resistance	$r_{DS(on)}$	52m $\Omega$ (typ) 70m $\Omega$ (max)	$V_{GS} = 10V, I_D = 15A$
Internal Gate Resistance	$R_{gint}$	1 $\Omega$	$f = 1MHz$ , Open drain
Gate-Drain Charge	$Q_{GD}$	4nC	$V_{DS} = 75V, V_{GS} = 10V, I_D = 15A$
	$g_m$	14.86643	125 $^{\circ}C$
	$g_m$	23.70255	25 $^{\circ}C$

Table 1. Electrical parameters for MCAC15N15Y relevant for calculations.

The parameters referent to device driving are switching frequency

$$f_{sw} = 10kHz = \frac{1}{T} = \frac{1}{0.1ms} \text{ and the duty cycle } D = 80\%.$$

Firstly, it is necessary to calculate equivalent capacitance with

$$C_{GD} = \frac{4nC}{75V - 15A(52m\Omega)} = \frac{4nC}{74.22} = 53.8938pF.$$

The  $C_{oss}$  is obtained simply using the parameter  $E_{oss} = 388.11037nJ$  extracted from simulation like

$$C_{oss} = \frac{2(388.11037nJ)}{(75V - 15A(52m\Omega))^2} = 140.9105pF,$$

$$C_{DS} = 140.9105pF - 53.8938pF = 87.0167pF.$$

The  $C_{iss}$  is taken directly from the datasheet as it's the only capacitance that remains with nearly linear behavior despite the voltage applied. For this example,  $C_{iss} = 740pF$ .

After that, it is now possible to calculate  $V_{pon}$  and  $V_{poff}$  with equation below. The result is

$$V_{gp-ON} = \frac{V_{th}g_mR_gC_{GD} + I_oR_gC_{GD} + V_{GG}(C_{GD} + C_{DS})}{(1 + g_mR_g)C_{GD} + C_{DS}}$$

$$V_{gp-OFF} = \frac{V_{th}g_mR_gC_{GD} + I_oR_gC_{GD}}{(1 + g_mR_g)C_{GD} + C_{DS}}$$

$$V_{gp-ON} = \frac{3V(14.866)(11\Omega)(53.894pF) + 15A(11\Omega)(53.894pF)}{53.894pF(1 + 14.866(11\Omega)) + 87.0167pF} + \frac{10V(53.894pF + 87.0167pF)}{53.894pF(1 + 14.866(11\Omega)) + 87.0167pF} = 4.1033V,$$

$$V_{gp-OFF} = \frac{3V(14.866)(11\Omega)(53.894pF) + 15A(11\Omega)(53.894pF)}{53.894pF(1 + 14.866(11\Omega)) + 87.0167pF} = 3.9459V$$

Now, the calculation for the times intervals  $t_{ON}$  and  $t_{OFF}$  is written as

$$t_{ON} = R_G \cdot C_{iss} \cdot \ln\left(\frac{V_{GG} - V_{th}}{V_{GG} - V_p}\right) + R_G \cdot C_{GD_{Av}} \left(\frac{V_{DD} - I_0 r_{DS(on)}}{V_{GG} - V_p}\right),$$

$$t_{OFF} = R_G \cdot C_{GD_{Av}} \left(\frac{V_{DD} - I_0 r_{DS(on)}}{V_p}\right) + R_G \cdot C_{iss} \cdot \ln\left(\frac{V_p}{V_{th}}\right).$$

$$t_{ON} = 11\Omega \left[ (740pF) \ln\left(\frac{10V - 3V}{10V - 4.1033V}\right) + 53.8938pF \left(\frac{75V - 21A(52m\Omega)}{10V - 4.1033V}\right) \right]$$

$$= 8.8579ns,$$

$$t_{OFF} = 11\Omega \left[ (53.8938pF) \left(\frac{75V - 15A(52m\Omega)}{3.9459V}\right) + (740pF) \ln\left(\frac{3.9459V}{3V}\right) \right]$$

$$= 13.3817ns.$$

Following with the process described in the document, now it is possible to calculate the energy dissipated due to switching of the transistor:

$$E_{on} = \frac{1}{2} 15A(75V)(8.8579ns) = 4.9826\mu J,$$

$$E_{off} = \frac{1}{2} 15A(75V)(13.3817ns) = 7.5272\mu J,$$

$$E_{oss} = 0.3881104\mu J$$

and then get the average power dissipation by multiplying by the switching frequency like

$$P_{sw_{av}} = [E_{on} + E_{off} + E_{oss}] f_{sw}$$

$$= [4.9826\mu J + 7.5272\mu J + 0.3881104\mu J](10kHz) = 0.129W.$$

Conduction and driver power losses are also included in the average power losses of the device. Using the values from the datasheet and application circuit we have

$$P_{Cond} = (15A)^2(52m\Omega)(0.8) = 9.36W,$$

$$P_{Driver} = 10V(13nC)(10kHz) = 1.3mW.$$

Thus, the total average power losses due to MOSFET are

$$P_{MOS} = 9.25W + 196.193mW + 1.8mW = 9.448W$$

## 5. Simulation

Calculations using datasheets values shown in Table 1 and Table 2 were used to calculate results in Table 4.

	$t_{ON} = t_{21_{ON}} + t_{32_{ON}}$	$t_{OFF} = t_{21_{OFF}} + t_{32_{OFF}}$	Power Losses
<i>Simulation</i>	9.86ns	8.17ns	9.4324W
<i>Calculation</i>	8.8579ns	13.3817ns	9.448mW

Table 2. Comparison between simulation and calculation results of switching times and power losses for MCAC15N15Y.

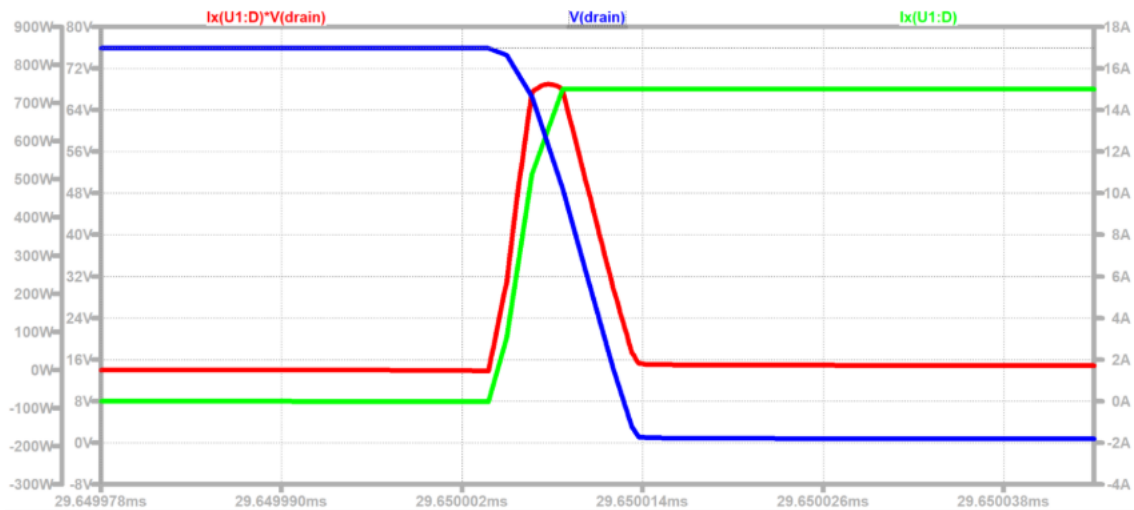


Figure 7. Turn-ON waveform for MCAC15N15Y in Itspice. The red waveform corresponds to the power losses due to the switching between ON and OFF.

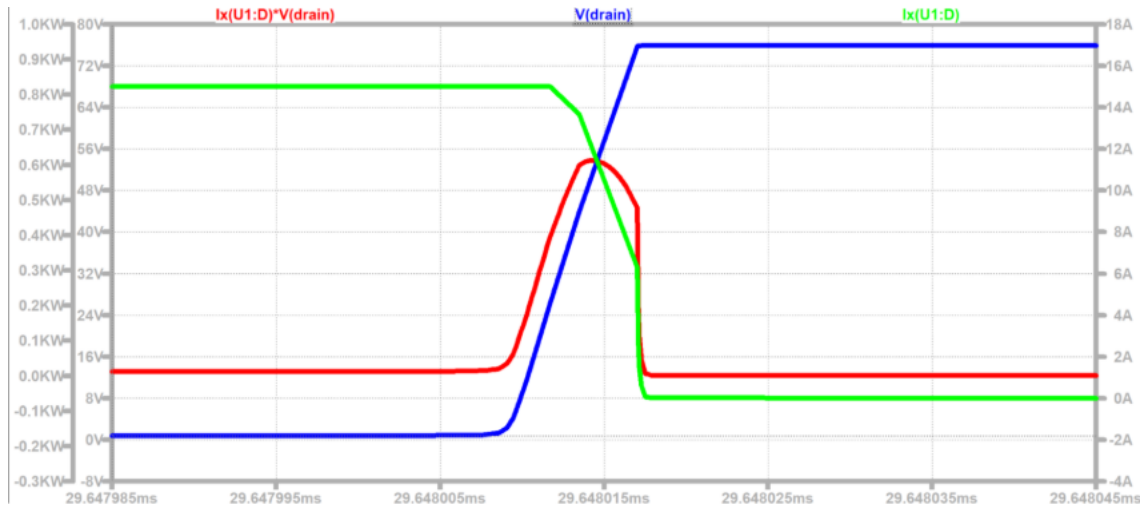


Figure 8. Turn-OFF waveform for MCAC15N15Y in its spice. The red waveform corresponds to the power losses due to the switching between OFF and ON.

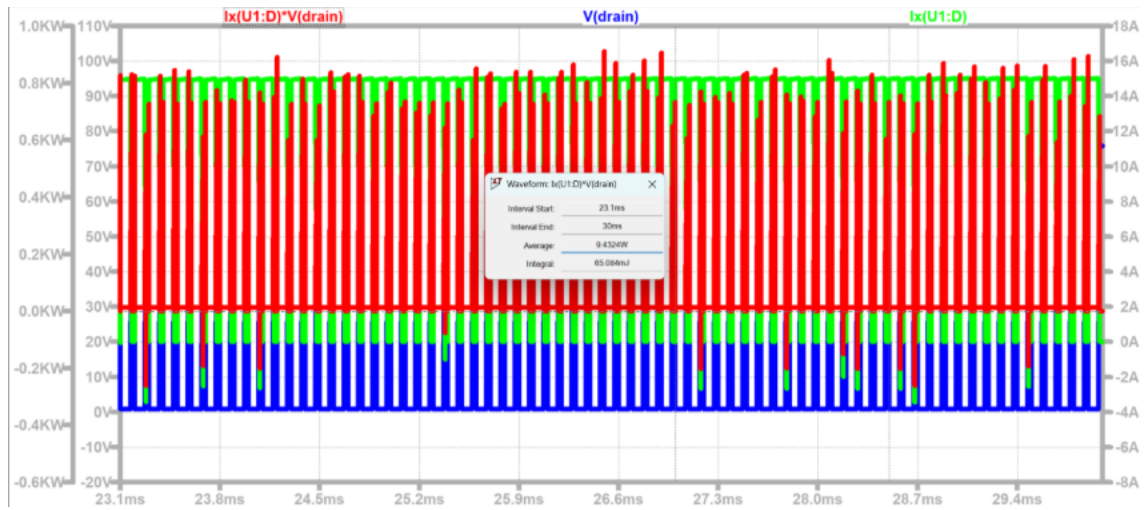


Figure 9. Average power losses for the MCAC15N15Y.

## 6. Conclusions

In this application note, a calculation approach for estimating total losses in power MOSFET switching applications was presented. With this approach, conduction and switching losses can be evaluated and compared during component selection. Achieving low  $R_{DS(on)}$  while maintaining strong dynamic characteristics is often a design trade-off, and this analysis helps determine the optimal balance.

Additionally, the procedure presented here allows designers to identify the main contributors to switching losses, including transition times where drain-to-source voltage and current overlap, output capacitance discharge, and gate driving losses. This becomes increasingly important as switching frequencies continue to rise due to the industry trend toward higher power density.

Finally, a simulation example was presented to demonstrate how closely this simplified analysis matches full electrical model simulations, allowing the approach to be used for worst-case analysis and component comparisons without significantly compromising accuracy.

## References

- [1] Erickson, R. W., & Maksimović, D. (2020, p. 123). *Fundamentals of Power Electronics* (3.ª ed.). Springer. <https://doi.org/10.1007/978-3-030-43881-4>.
- [2] MCC. (2026). Application Note: Quick guide for power losses calculation in MOSFETS – Part 2. Micro Commercial Components Corp. <https://solutions.mccsemi.com/news/application-note-quick-guide-for-power-losses-calculation-in-mosfets-part-2>. Section 2.2
- [3] I. Zeltser and S. Ben-Yaakov, "On SPICE Simulation of Voltage-Dependent Capacitors," in *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3703-3710, May 2018, doi: 10.1109/TPEL.2017.2766025.
- [4] Sam Ben-Yaakov. (2018, 24 enero). *Deciphering Coss of power MOSFETs* [Vídeo]. YouTube. <https://www.youtube.com/watch?v=4bGbthmT5MQ>
- [5] U. Jadli, F. Mohd-Yasin, H. A. Moghadam, J. R. Nicholls, P. Pande and S. Dimitrijević, "A Simple Equation for the Energy Stored by Voltage-Dependent Capacitances," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 12629-12632, Dec. 2020, doi: 10.1109/TPEL.2020.2993639.