Micro Commercial Components

APPLICATION NOTE

Quick Guide for Power Losses Calculation in MOSFETS – Part 2

Approach to Estimate Switching Time Intervals Using Datasheet Parameters

In Part I of this application note series, a practical framework was introduced to estimate switching power losses in Power MOSFETs by calculating turn-ON and turn-OFF time intervals. These equations provide a useful first-order method for evaluating switching behavior in hard-switching applications using a simplified driver model.

However, applying these equations in real design scenarios quickly reveals a common challenge: several key parameters required for the calculations are strongly dependent on operating conditions and are not always directly available from datasheets in a form suitable for comparison.

This second part of the series addresses that gap.

1. Introduction

In Part I of this series, equations were developed to calculate MOSFET turn ON and turn OFF switching time intervals. These time intervals form the basis for switching power loss calculations in hard switching applications.

When applying these equations, it becomes evident that additional guidance is required. Several parameters used in the calculations, particularly gate plateau voltage and parasitic capacitances, depend strongly on operating voltage and current conditions. These parameters are not always directly available for the intended use case.

This application note provides practical methods to estimate these parameters using commonly available datasheet information. Approaches for plateau voltage approximation, reverse transfer capacitance extraction, and output capacitance modeling are presented. These methods enable consistent comparison of MOSFET switching behavior across suppliers when detailed SPICE models are not available.

The techniques described in this **Part II** are intended for component level comparison and early-stage device selection. When the objective is application-level loss modeling or worst-case analysis, time domain simulation using validated SPICE models remains the preferred approach.

1.1 ON and OFF time intervals

From Part I of this series, time intervals for the turn-ON transition are given as follows:

$$t_{10_{ON}} = \tau \ln\left(\frac{V_{GG}}{V_{GG} - V_{th}}\right)$$

Formula 1

$$t_{21_{ON}} = \tau \ln\left(\frac{V_{GG} - V_{th}}{V_{GG} - V_{gp-ON}}\right)$$

Formula 2

$$t_{32_{ON}} = R_G C_{GD} \frac{V_{DD} - I_o r_{DS_{(on)}}}{V_{GG} - V_{gp-ON}}$$

Formula 3

In addition, the turn-OFF transition time intervales were found to be:

$$t_{10_{OFF}} = \tau \ln\left(\frac{V_{GG}}{V_{gp-OFF}}\right)$$

Formula 4

$$t_{21_{OFF}} = R_G C_{GD} \frac{V_{DD} - I_o r_{DS_{(on)}}}{V_{gp-OFF}}$$

Formula 5

$$t_{32_{OFF}} = \tau \ln\left(\frac{V_{gp-OFF}}{V_{th}}\right)$$

Formula 6

Where $\tau = R_G(C_{GS} + C_{GD})$, the time intervals are defined as in Figure 1, and the following parameter definition apply:

- $\mathbf{R_G}$: Gate resistance (internal and external).
- $\mathbf{C_{GS}}$: Parasitic Gate-to-Source Capacitance.
- $\mathbf{C_{GD}}$: Parasitic Gate-to-Drain Capacitance.
- $\mathbf{R_{DS_{(on)}}}$: Drain-to-Source resistance when MOSFET is fully-ON.
- $\mathbf{V_{th}}$: Threshold Voltage.
- $\mathbf{V_{gp-ON}}$: Plateau Voltage during ON transition.
- $\mathbf{V_{gp-OFF}}$: Plateau Voltage during OFF transition.
- $\mathbf{V_{GG}}$: Gate external voltage supply DC value.
- $\mathbf{V_{DD}}$: Drain external voltage supply DC value.
- $\mathbf{I_o}$: Drain load DC current.

Formulas 1-6 were derived from a Low-Side Driver sample circuit with inductive load and ideal recirculating diode as the one shown in Figure 2

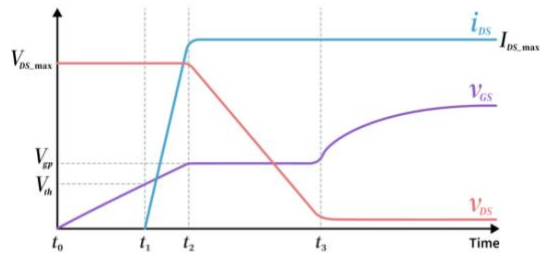
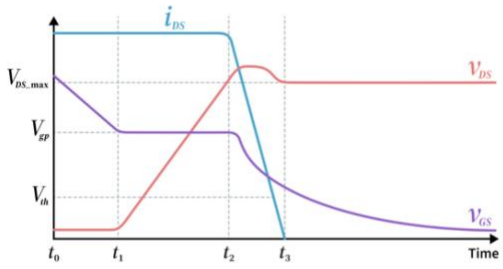
Figure 1a: Turn-On MOSFET Waveforms	Figure 1b: Turn-Off MOSFET Waveforms
	

Figure 1 – Switching Transition Waveforms

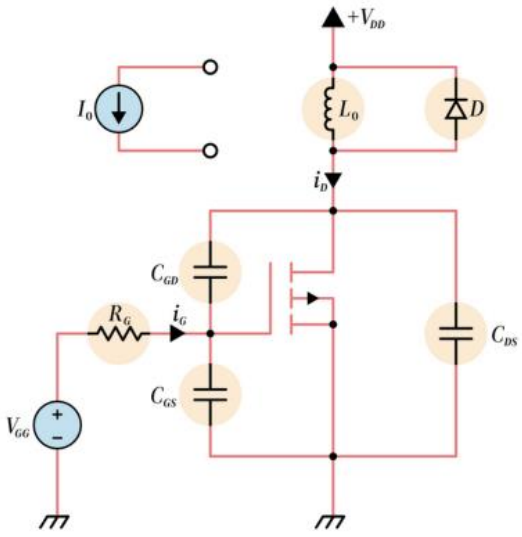


Figure 2 – Low-Side Driver Sample Circuit

2. Parameter approximations

2.1 Plateau Voltage for ON and OFF stages

It is clear from equations 2-4 and 6 that Gate Plateau Voltage is a parameter of high importance. However, deciding what voltage to use is often difficult.

Datasheet will show a Plateau Voltage under a determined set of conditions of Drain Voltage and Current. This value can be extracted from the datasheet Gate Charge plot to be used for calculations (Figure 3).

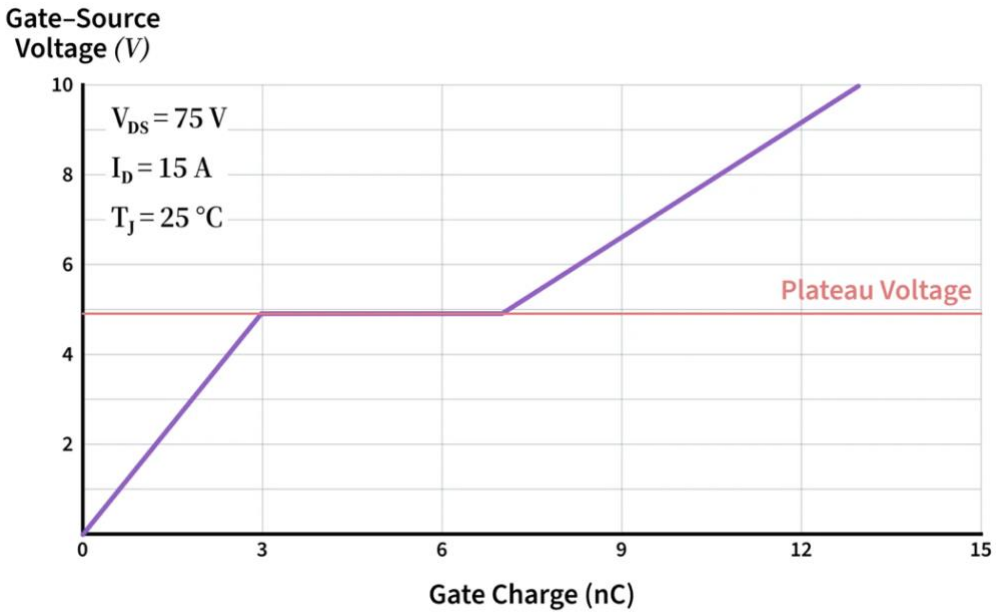


Figure 3 – Typical Gate Charge plot from Power MOSFET datasheet

Nevertheless, conditions for measuring Plateau Voltage are not standard and therefore looking for an approximation that considers surrounding conditions makes sense.

According to [1] Plateau Voltage might even be different depending if the device is turning OFF or turning ON, and it will be defined by the following equations:

$$V_{gp-ON} = \frac{V_{th} g_m R_g C_{GD} + I_o R_g C_{GD} + V_{GG}(C_{GD} + C_{DS})}{(1 + g_m R_g) C_{GD} + C_{DS}}$$

Formula 7

$$V_{gp-OFF} = \frac{V_{th} g_m R_g C_{GD} + I_o R_g C_{GD}}{(1 + g_m R_g) C_{GD} + C_{DS}}$$

Formula 8

Where $g_m$is the transconductance obtained from the slope of the linear portion of the Transfer Characteristics (Figure 4).

Equations 7 and 8 are an option to derive Plateau Voltages for ON and OFF stages that bring datasheet Plateau to closer reference conditions for parameter comparison of two or more Power MOSFET Part-Numbers.

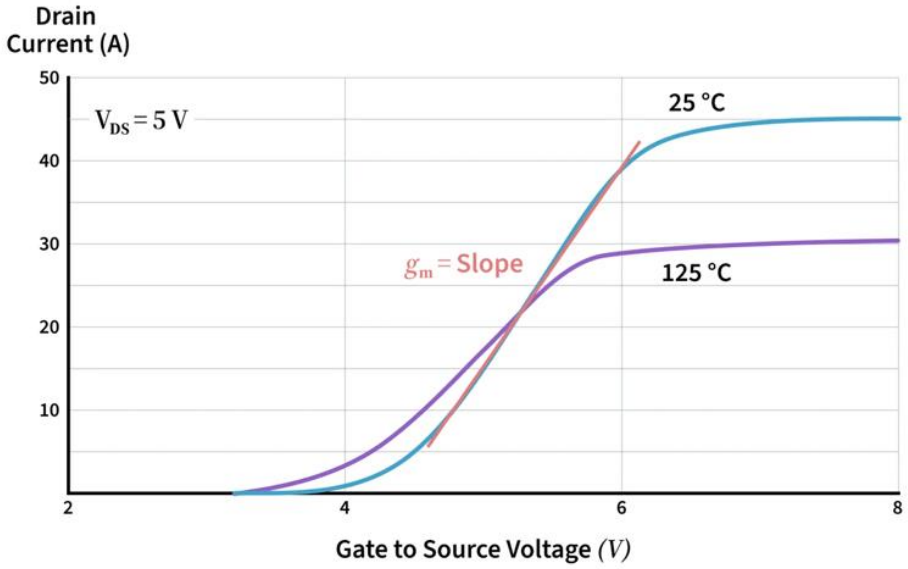


Figure 4 – Typical Transfer Characteristics Plot from Power MOSFET datasheet

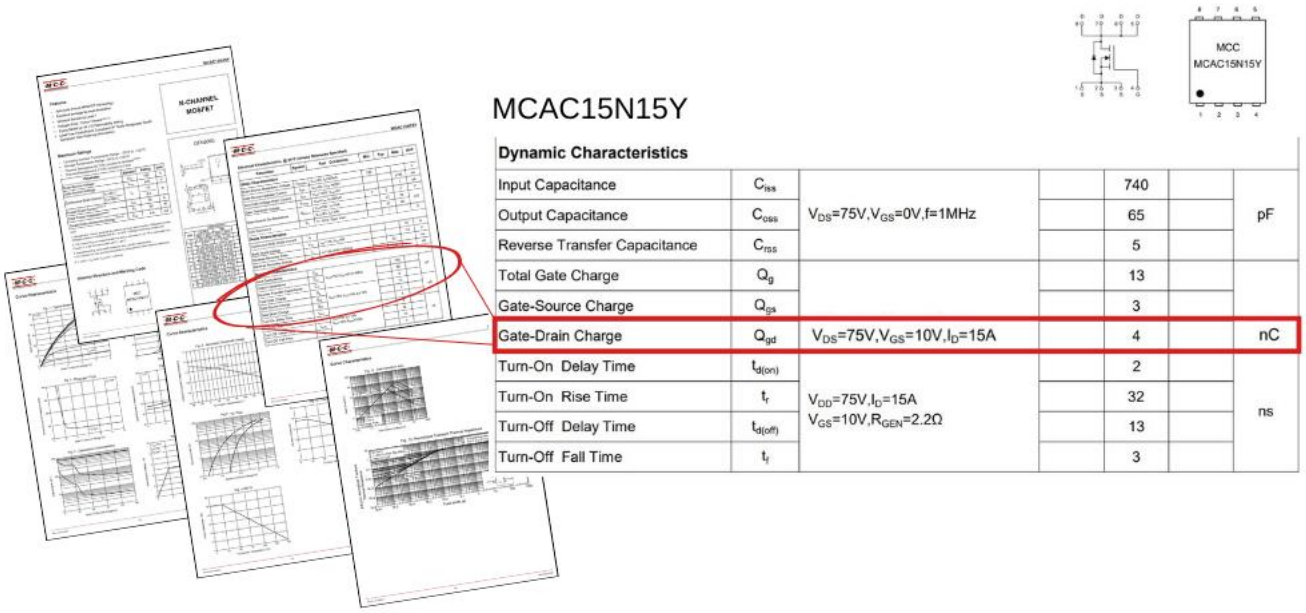
2.2. Reverse Transfer Capacitance (C_{rss})

From Part I of this series, we know that Reverse Transfer Capacitance C_{rss} is equal to C_{GD} which is a major parameter for equations 3 and 5. C_{GD} can be obtained by using Gate-Drain charge, Q_{GD}, from datasheet dynamic characteristic tables, which lets the following formula to be applied:

$$C_{GD} = \frac{Q_{GD}}{V_{DS_{swing}}}$$

Formula 9

When using this method, it needs to be considered that Q_{GD} is obtained with a determined V_{GS} value different from zero and that C_{GD} non-linear capacitor is both dependent on V_{GS} and V_{DS} bias values (Figure 5).


MCAC15N15Y

Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V,f=1MHz		740		pF
Output Capacitance	C_{oss}			65		
Reverse Transfer Capacitance	C_{rss}			5		
Total Gate Charge	Q_g			13		nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}	V_{DS}=75V,V_{GS}=10V,I_D=15A		4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=75V,I_D=15A V_{GS}=10V,R_{GEN}=2.2Ω		2		ns
Turn-On Rise Time	t_r			32		
Turn-Off Delay Time	$t_{d(off)}$			13		
Turn-Off Fall Time	t_f			3		

Figure 5. Example of Gate-Drain Charge from Power MOSFET Datasheet

Another way of approaching this capacitance will let us have values obtained from a standard method [3] that uses same measurement conditions making component comparison more trustable. C_{rss} characteristics plot, Figure 6, is obtained with a sweep of bias voltages for V_{DS} with added small signal vds high frequency disturbances (i.e. capacitances in Figure 6 are small signal capacitances). It is worth noting that is an industry standard to have $V_{GS} = 0V$ during this characterization.

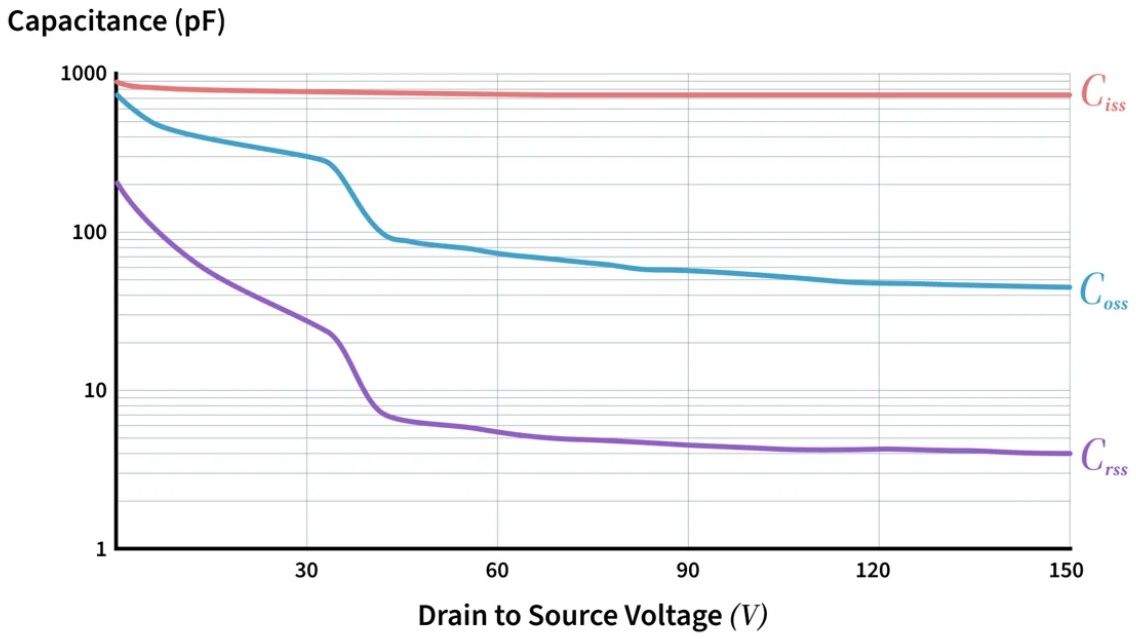


Figure 6 – Example MOSFET Small-Signal Capacitance plots from Datasheet

From this plot, we can read the $C_{rss} = C_{GD}$ value to desired V_{DS} voltage and use it for time interval calculations. That is one valid way of doing it, sufficiently good for comparison purposes.

Alternative way is to find an equivalent linear capacitor value related to the charge on the non-linear capacitor at the desired V_{DS}. To do this, all points in the C_{rss} capacitance characteristics need to be extracted and used to simulate the non-linear charge curve with respect to its terminal voltages

using the method in [2]. C_{GD} is then obtained applying formula (9). These last two methods allow us to have C_{GD} values for all MOSFETs in comparison that use the same V_{DS} and V_{GS} bias conditions.

This last simulation step can be regarded as an unnecessary extra step if the analysis goal is just to compare component performance. However, having this simulation allows detailing the non-linear capacitors more completely as is shown in Figure 7.

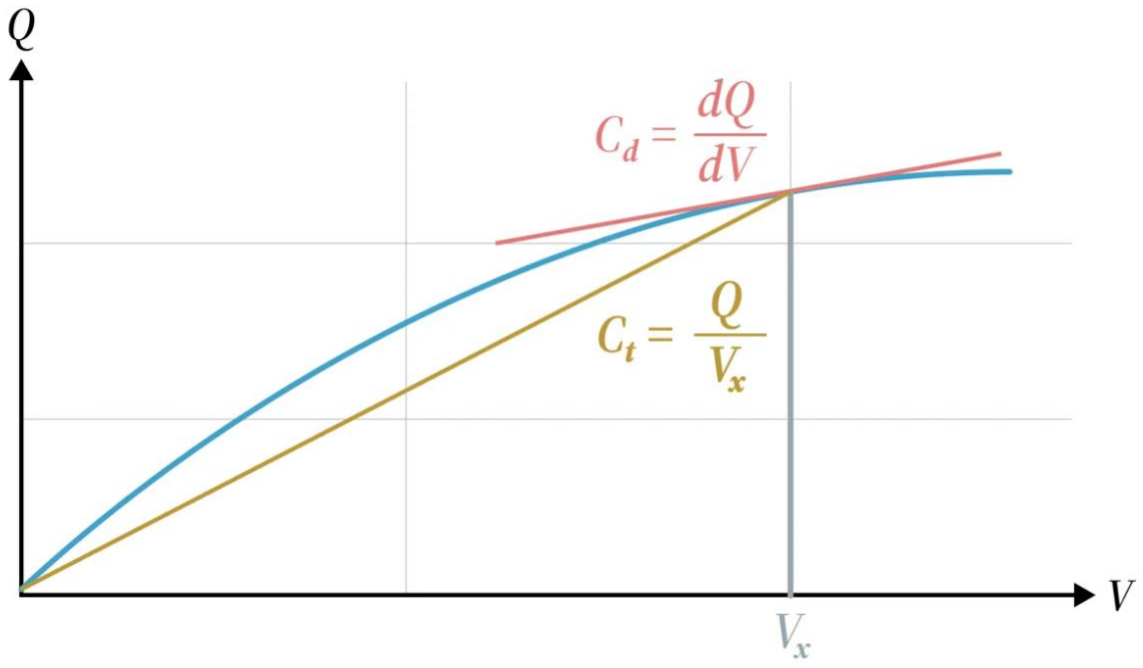


Figure 7 – Non-linear capacitor charge curve (C_d – small signal capacitance at Vx, C_t – equivalent linear capacitor at Vx)

2.3 Output Capacitance (C_{oss})

Once $C_{GD}$is defined, the same approach can be taken for C_{DS}. In similarity with C_{rss}, Output Capacitance C_{oss} is defined in Figure 6 plot. Same benefit of having measurements with a well stablished method is accomplished, this makes conditions between suppliers similar and comparable.

The value of C_{DS} is obtained after applying the following subtraction:

$$C_{DS} = C_{oss} - C_{GD}$$

Formula 10

Where, as was detailed above, C_{oss} can be read directly from the small signal non-linear capacitance plot (Figure 5) or the points from this characteristic can be extracted to simulate the non-linear charge curve with respect to Drain-to-Source voltage [2] and use:

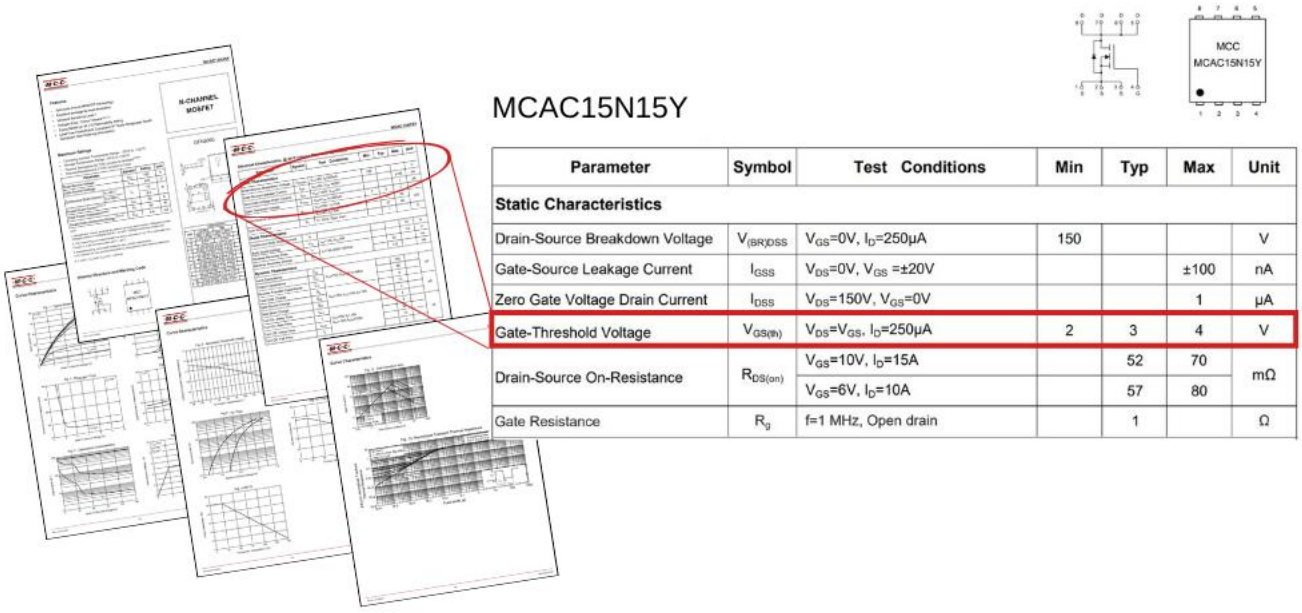
$$C_{DS} = \frac{Q_{OSS}}{V_{DS_{swing}}} - C_{GD}$$

Formula 11

2.4 Gate-Threshold Voltage (V_{th})

For this Application Note, typical Threshold Voltage defined from the datasheet is used. No detailed calculation was found in the literature.

In addition, vendors typically use the same conditions (i.e. $V_{DS} = V_{GS}$, $I_D = 250\mu A$) for measuring this parameter which makes comparison easier (Figure 8).



MCAC15N15Y

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	150			V
Gate-Source Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V, V_{GS}=0V			1	μA
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2	3	4	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=15A		52	70	mΩ
		V_{GS}=6V, I_D=10A		57	80	
Gate Resistance	R_g	f=1 MHz, Open drain		1		Ω

Figure 8. Typical Gate-Threshold Datasheet table

3 Calculation example

3.1 Sample circuit

Taking the following values for surrounding conditions on Figure 1 Low-Side driver circuit: $V_{GG} = 10V, V_{DD} = 75V, I_o = 15A, R_{g_{ext}} = 10\Omega$ an example calculation will be presented here.

For this MCC's Power MOSFET MCAC15N15Y will be used along with two competitor MOSFETs that are close in electrical characteristics. Table 1 and Table 2 show these component parameters that are relevant for this analysis.

Parameter	Symbol	MCAC15N15Y	Conditions
Drain-Source Maximum Voltage	V_{DS}	150V	$V_{GS} = 0V, I_D = 250\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	2V to 4V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source On-Resistance	$r_{DS_{(on)}}$	52mΩ (typ) 70mΩ (max)	$V_{GS} = 10V, I_D = 15A$
Internal Gate Resistance	R_{gint}	1Ω	$f = 1MHz$, Open drain
Gate-Drain Charge	Q_{GD}	4nC	$V_{DS} = 75V, V_{GS} = 10V, I_D = 15A$
Plateau-Voltage	V_p	4.9V	$V_{DS} = 75V, I_D = 15A$
Input Capacitance	$C_{iss} = C_{GS} + C_{GD}$	749.9pF	$V_{DS} = 30V, V_{GS} = 0V, f = 1MHz$
Output Capacitance	$C_{oss} = C_{DS} + C_{GD}$	301.1pF	$V_{DS} = 30V, V_{GS} = 0V, f = 1MHz$
Reverse Transfer Capacitance	$C_{rss} = C_{GD}$	27.3pF	$V_{DS} = 30V, V_{GS} = 0V, f = 1MHz$

Table 1. Electrical parameters for MCAC15N15Y relevant for calculations.

Symbol	Competitor A	Conditions	Competitor B	Conditions
V_{DS}	200V	$V_{GS} = 0V, I_D = 250\mu A$	150V	$V_{GS} = 0V, I_D = 250\mu A$
$V_{GS(th)}$	2V to 4V	$V_{DS} = V_{GS}, I_D = 1mA$	2V to 4V	$V_{DS} = V_{GS}, I_D = 35\mu A$
$r_{DS_{(on)}}$	86mΩ (typ) 102mΩ (max)	$V_{GS} = 10V, I_D = 12A$	42mΩ (typ) 52mΩ (max)	$V_{GS} = 10V, I_D = 18A$
R_{gint}	1.1Ω	$f = 1MHz$	2.1Ω	$f = 1MHz$
Q_{GD}	10.1nC	$V_{DS} = 100V, V_{GS} = 10V, I_D = 12A$	1.5nC	$V_{DS} = 75V, V_{GS} = 10V, I_D = 9A$
V_p	4.5V	$V_{DS} = 100V, I_D = 12A$	5.2V	$V_{DS} = 75V, I_D = 9A$
$C_{iss} = C_{GS} + C_{GD}$	1568pF	$V_{DS} = 30V, V_{GS} = 0V,$ $f = 1MHz$	670pF	$V_{DS} = 75V, V_{GS} = 0V,$ $f = 1MHz$
$C_{oss} = C_{DS} + C_{GD}$	170pF	$V_{DS} = 30V, V_{GS} = 0V,$ $f = 1MHz$	80pF	$V_{DS} = 75V, V_{GS} = 0V,$ $f = 1MHz$
$C_{rss} = C_{GD}$	55pF	$V_{DS} = 30V, V_{GS} = 0V,$ $f = 1MHz$	3.4pF	$V_{DS} = 75V, V_{GS} = 0V,$ $f = 1MHz$

Table 2: Electrical parameters for competition that are relevant for calculations

3.2 LTspice simulation of sample circuit

Simulations using SPICE models from MCAC15N15Y and Competition were performed. From simulation results measured time intervals $t_{ON} = t_{21_{ON}} + t_{32_{ON}}$ and $t_{OFF} = t_{21_{OFF}} + t_{32_{OFF}}$ are going to be used in this analysis as a reference. Results are shown in Table 3. Figure 9 shows t_{ON} measurement from simulations taken from the point where the 5% of maximum Drain current is reached $(0.05 * I_o = 0.75A)$ to the point where 5% of the maximum Drain voltage is reached $(0.05 * V_{DD} = 3.75V)$. Same points, but with voltage appearing first than current were taken to measure t_{OFF} (Figure 10).

	MCAC15N15Y	Competitor A	Competitor B	Δ (MCC – Competition)	
				A	B
$t_{ON} = t_{21_{ON}} + t_{32_{ON}}$	8.68ns	18.40ns	5.46ns	**-9.72ns**	**3.22ns**
$t_{OFF} = t_{21_{OFF}} + t_{32_{OFF}}$	12.43ns	23.00ns	5.91ns	**-10.57ns**	**6.52ns**

Table 3. Turn-on and turn-off times obtained from simulation measurements

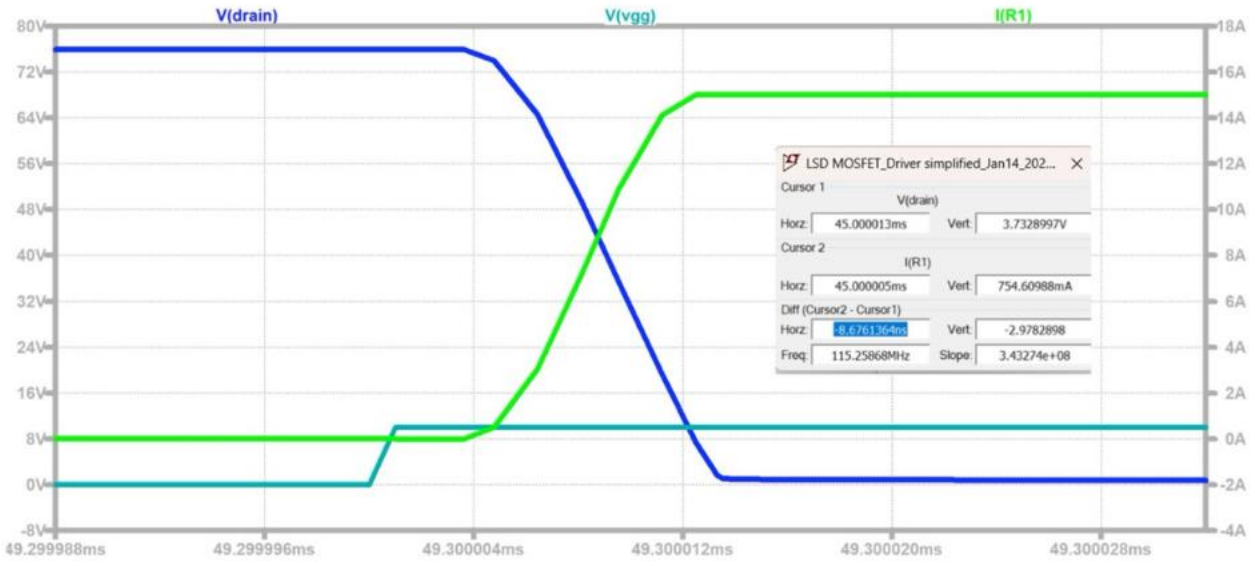


Figure 9. MCAC15N15Y Turn-on time from Simulation (I_o in green, V_{DS} in dark blue & V_{GG} in light blue

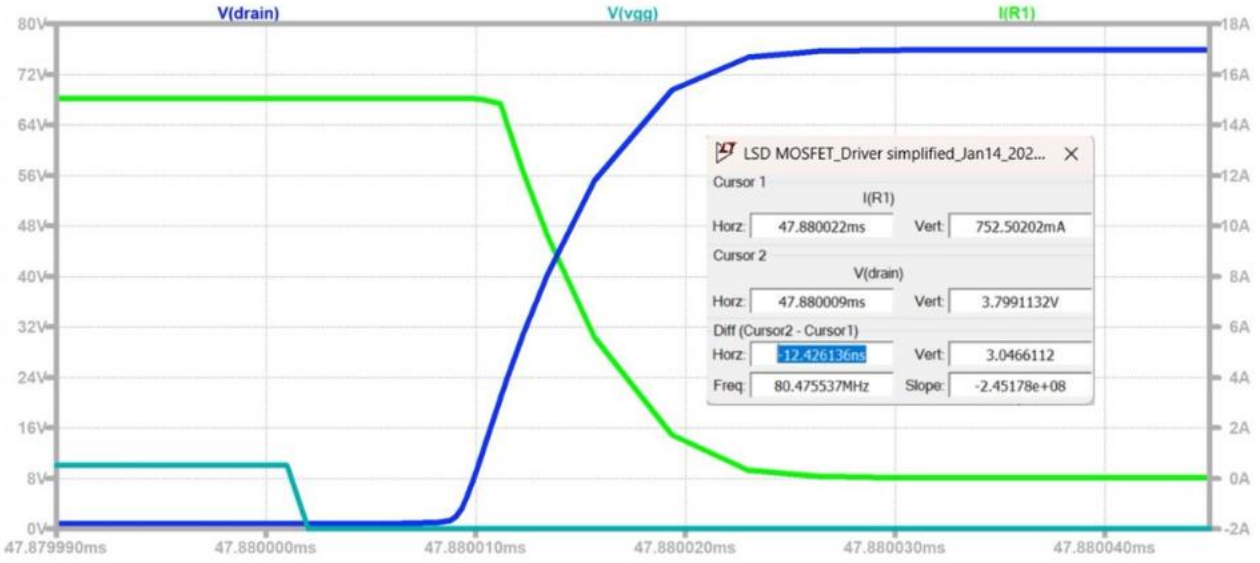


Figure 10. MCAC15N15Y Turn-off time from Simulation (I_o in green, V_{DS} in dark blue & V_{GG} in light blue)

3.3 Calculation using datasheet values

Calculations using datasheets values shown in Table 1 and Table 2 were used to calculate results in Table 4.

	MCAC15N15Y	Competitor A	Competitor B	Δ (MCC – Competition)	
				A	B
$t_{10_{ON}}$	2.94ns	6.26ns	2.91ns	--	--
$t_{21_{ON}}$	2.61ns	4.24ns	3.08ns	--	--
$t_{32_{ON}}$	4.37ns	8.26ns	2.02ns	--	--
$t_{ON} = t_{21_{ON}} + t_{32_{ON}}$	**6.98ns**	**12.49ns**	**5.1ns**	**-5.51ns**	**1.88ns**
$t_{10_{OFF}}$	5.89ns	14.02ns	5.33ns	--	--
$t_{21_{OFF}}$	4.55ns	10.09ns	1.87ns	--	--
$t_{32_{OFF}}$	4.05ns	7.12ns	4.48ns	--	--
$t_{OFF} = t_{21_{OFF}} + t_{32_{OFF}}$	**8.60ns**	**17.21ns**	**6.35ns**	**-8.61ns**	**2.25ns**

Table 4: Calculation results using datasheet values

3.4 Calculation using Plateau Voltage

Modeling approach of Plateau Voltage described in Section 2.1 was used to obtain results shown in Table 5.

	MCAC15N15Y	Competitor A	Competitor B	Δ (MCC – Competition)	
$t_{10_{ON}}$	2.94ns	6.33ns	2.91ns	--	--
$t_{21_{ON}}$	1.22ns	1.35ns	1.80ns	--	--
$t_{32_{ON}}$	3.69ns	7.00ns	1.73ns	--	--
$t_{ON} = t_{21_{ON}} + t_{32_{ON}}$	**4.91ns**	**8.35ns**	**3.52ns**	**-3.44ns**	**1.39ns**
$t_{10_{OFF}}$	8.60ns	18.78ns	8.99ns	--	--
$t_{21_{OFF}}$	6.32ns	13.23ns	2.92ns	--	--
$t_{32_{OFF}}$	1.33ns	2.36ns	0.82ns	--	--
$t_{OFF} = t_{21_{OFF}} + t_{32_{OFF}}$	**7.65ns**	**15.59ns**	**3.75ns**	**-7.94ns**	**3.90ns**

Table 5: Calculation results using Plateau Voltage model (Section 2.1)

Conclusions

Comparing switching performance of different Power MOSFET vendors or even same vendor Power MOSFET part numbers is always a challenge. Measurement conditions affect MOSFET parameters and this consequently affects any performance prediction.

However, in this application note we show that using Datasheet values or additional modeling approach of Plateau Voltage gives good results when targeting comparison, both will give a good approximation of how slow or how fast one component is against the other.

Delta comparisons between components using both approaches will give a good indication of how switching performance will perform when both are used under same conditions. Nevertheless, using the modeling approach of Plateau Voltage presented here will bring all comparisons to the same point of reference which is an added benefit if available specification of Plateau Voltage was taken under completely different conditions.

References

[1] Liu, S., Song, S., Xie, N., Chen, H., Wu, X., & Zhao, M. (2021). Miller Plateau Corrected with Displacement Currents and Its Use in Analyzing the Switching Process and Switching Loss. *Electronics 2021, 10*]

[2] Ben-Yaakov, S. & Zeltser, I. (2017). On SPICE simulation of voltage dependent capacitors. *IEEE Transactions in Power Electronics*

[3] JEDEC SOLID STATE TECHNOLOGY ASSOCIATION (1985). JESD24 JEDEC Standard for Power MOSFETs