Guide for Power Loss Calculations in MOSFETs

Part 1: An Approach to Estimate Switching Time Intervals in Power MOSFETs

Design engineers face a growing challenge in optimizing power efficiency in modern electronic systems, especially as applications demand faster switching speeds and higher performance. Whether in automotive control units, industrial motor drives, or consumer electronics, excessive power dissipation during switching events can lead to increased thermal stress, reduced reliability, and higher energy costs.

One of the most critical contributors to power loss in these systems is switching loss in MOSFETs. This becomes particularly significant in circuits involving inductive loads. Despite the widespread use of MOSFETs for their fast-switching capabilities and ease of control, accurately estimating and comparing switching losses across different components remains a complex task.

Focus here is on calculating switching times, which are essential for understanding dynamic power dissipation. MCC offers a range of Power MOSFETs optimized for switching applications (see **Table 1**). One of these parts will be used as a reference in the calculation and simulation examples presented in the following sections of this series

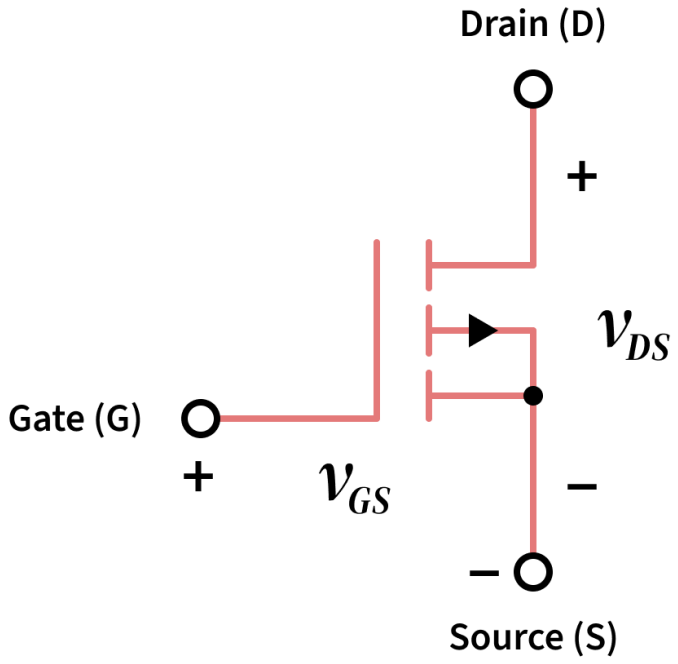
Table 1: **MCC Power MOSFET Line-Up for Switching Applications**

Part Number	Package	Type	V_{DS} (V)	RDS(ON) Max @VGS=10V (Ω)	Ciss(pF)	Coss(pF)	Crss(pF)	Qg(nC)
MCAC8D8N04YL	DFN5060	N	40	0.0088	681	296	6.6	12
MCG5D9N03YL	DFN3333	N	30	0.0059	594	491	43	12.4
MCAC5D5N03YL	DFN5060	N	30	0.0055	560	500	50	12.4
MCAC25N10YHE3	DFN5060	N	100	0.033	509	271	35	12.7
MCAC15N15Y	DFN5060	N	150	0.07	740	65	5	13

2: The Power MOSFET

The Power MOSFET is a voltage-controlled unipolar device that requires only a small amount of input (Gate, G) current (non-latching) to operate. The MOSFET will continue to allow current to flow between Drain (D) and Source (S) if the required amount of Gate (G) to Source (S) voltage, VGS, is maintained, as seen in **Figure-1**.

Figure 1: **Power MOSFET Terminal Diagram**

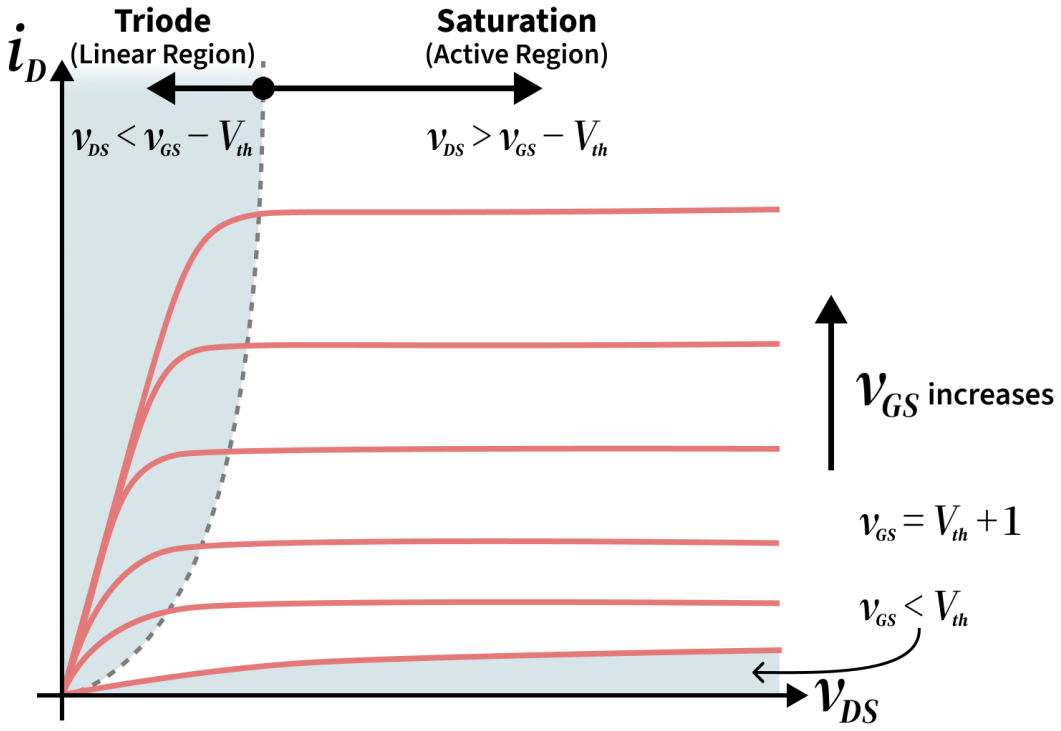


Since only majority carriers contribute to the current flow, MOSFETs have a high switching speed capability (exceeding several hundreds of kHz in practical applications).

2.1: Operation Modes of the MOSFET

For MOSFET to carry Drain current, a channel between the Drain and the Source must be created. This occurs when the Gate-to-Source exceeds the device threshold voltage (V_{th}). For $v_{GS} > V_{th}$ the device can be either in the triode region (constant resistance) or in the saturation region depending on the Drain to Source v_{DS} value as shown in **Figure-2**.

Figure 2: **Working regions of the MOSFET based on the i_D vs v_{DS} characteristic**

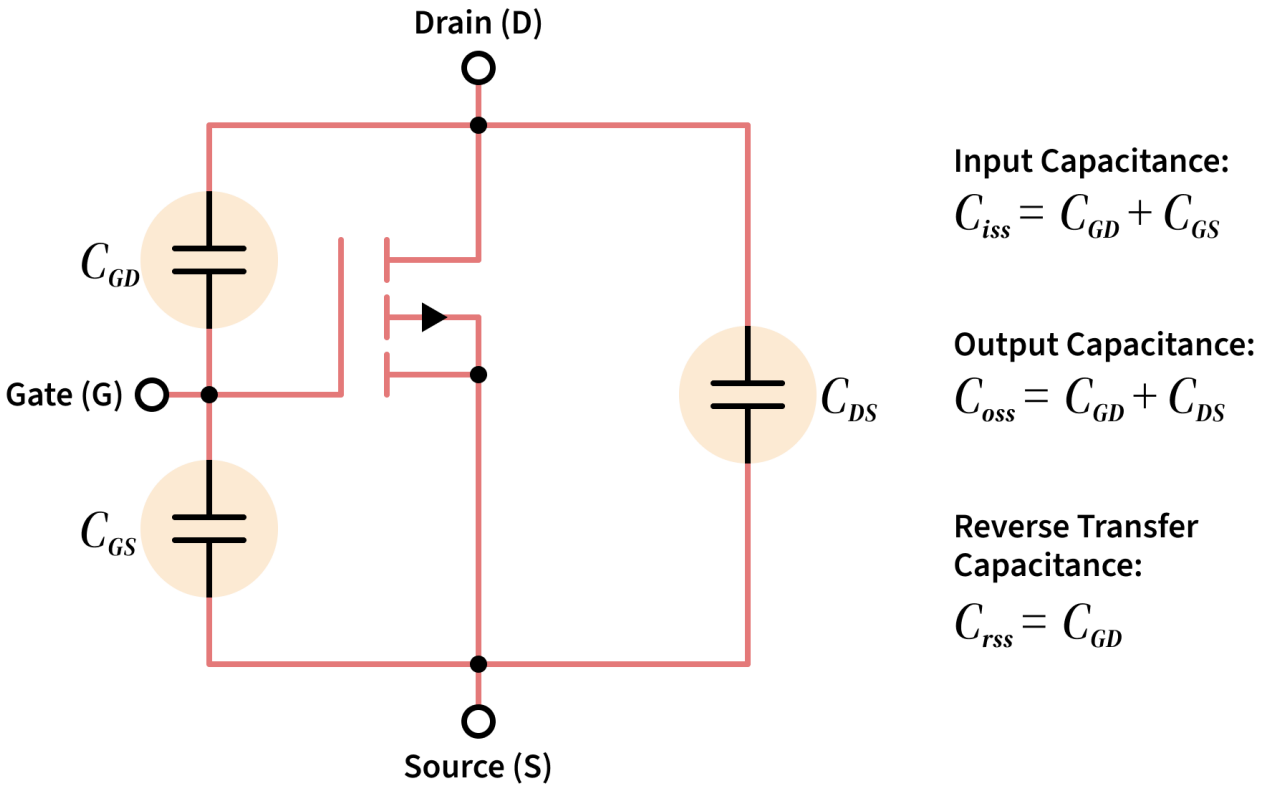


When the MOSFET is used as a switch, only triode and cut-off regions are used, whereas, when it is used as a controlled-current source, the MOSFET must operate in the saturation region.

2.2: Parasitic Capacitances of the MOSFET

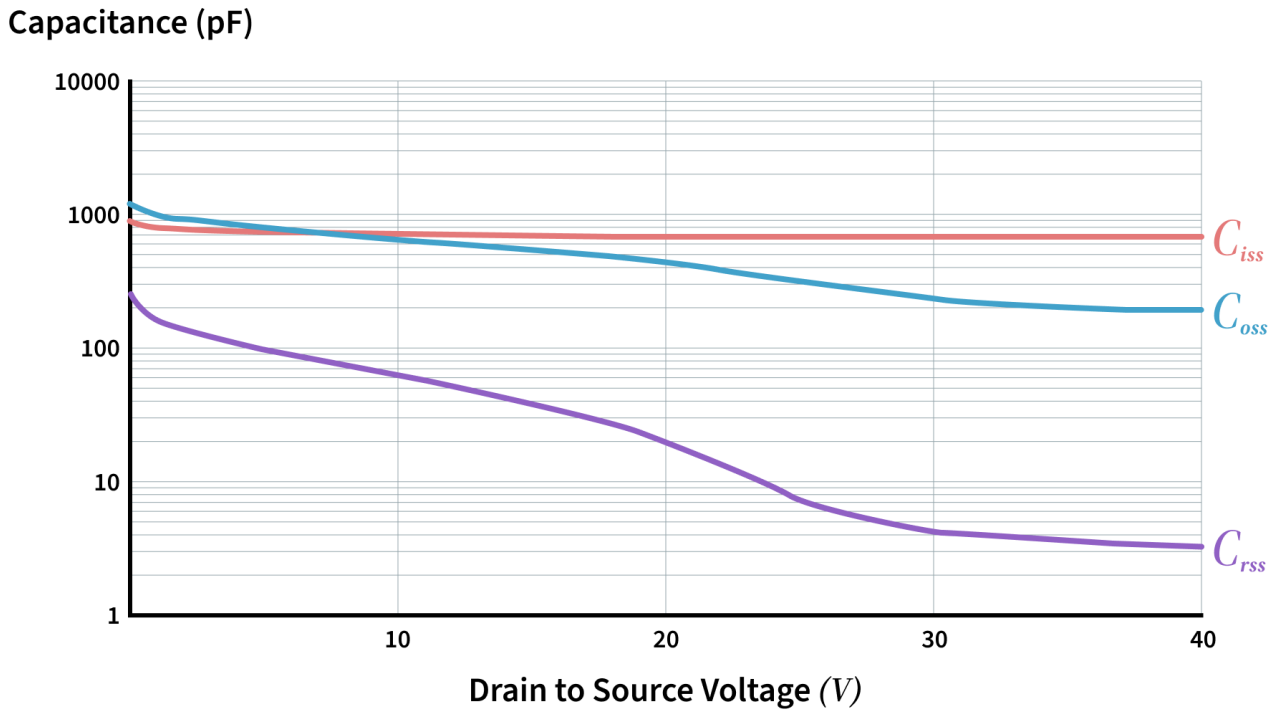
Parasitic Capacitances are important parameters that affect the MOSFET's switching behavior. They are located between the device's 3 terminals, namely: Gate-to-Source (C_{GS}), Gate-to-Drain (C_{GD}), and Drain-to-Source (C_{DS}) capacitances, see **Figure-3**.

Figure 3: **MOSFET Parasitic Capacitances**



The values of these capacitances are non-linear and a function of device structure, geometry and, particularly, of bias voltages. The MOSFET parasitic capacitances are given in terms of the typical device datasheet parameters (**Figure-4**) that are easier to measure C_{iss}, C_{oss} and C_{rss}. The relation is shown in **Figure-3** bottom equations.

Figure 4: **Typical Capacitance Plots of a MOSFET Datasheet**



3: Switching-Time Calculations (Turn-On and Turn-Off)

The turn-On and turn-Off processes of semiconductor devices are not discrete events; there will be a delay time between $i_{DS} = I_{DS\_MAX}$ (On state) and $i_{DS} \approx 0$ (Off state). According to the well known MOSFET switching behavior, these times can be divided into 3 different intervals of time, as can also be seen in the figures for turn-On and turn-Off events: **Figure-5a** and **Figure-5b**, respectively. In this document we will find a way of calculating:

- t_{ON_10}, turn-On delay time, which is the time it takes v_{GS} to reach V_{th}
- t_{ON_21}, turn-On rise-time, which is the time it takes drain current to go from $i_{DS} \approx 0$ to $i_{DS} = I_{DS\_MAX}$
- t_{ON_32}, turn-On plateau time, which is the time it takes the drain-source voltage v_{DS}, to go from its maximum value $v_{DS} = V_{DS\_MAX}$ to its ON-state voltage. Note that, during this time the v_{GS} remain at plateau value V_{gp-ON} (due to Miller effect).
- t_{OFF_10}, turn-Off delay time, or the time it takes v_{GS} to go from its maximum value to the plateau value V_{gp-OFF}.
- t_{OFF_21}, turn-Off plateau time, which is the time it takes v_{DS} to go from its ON-state voltage back to V_{DS_MAX}.
- t_{OFF_32}, turn-Off fall-time, which is the time it takes drain current to go from I_{DS_MAX} back to zero.

Figure 5a: **Turn-On MOSFET Waveforms**

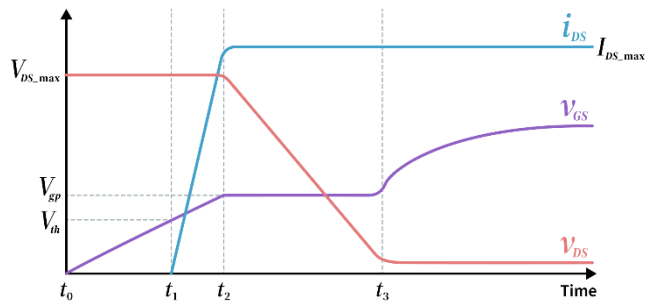
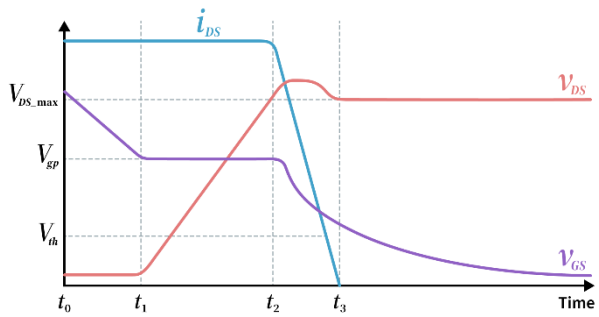
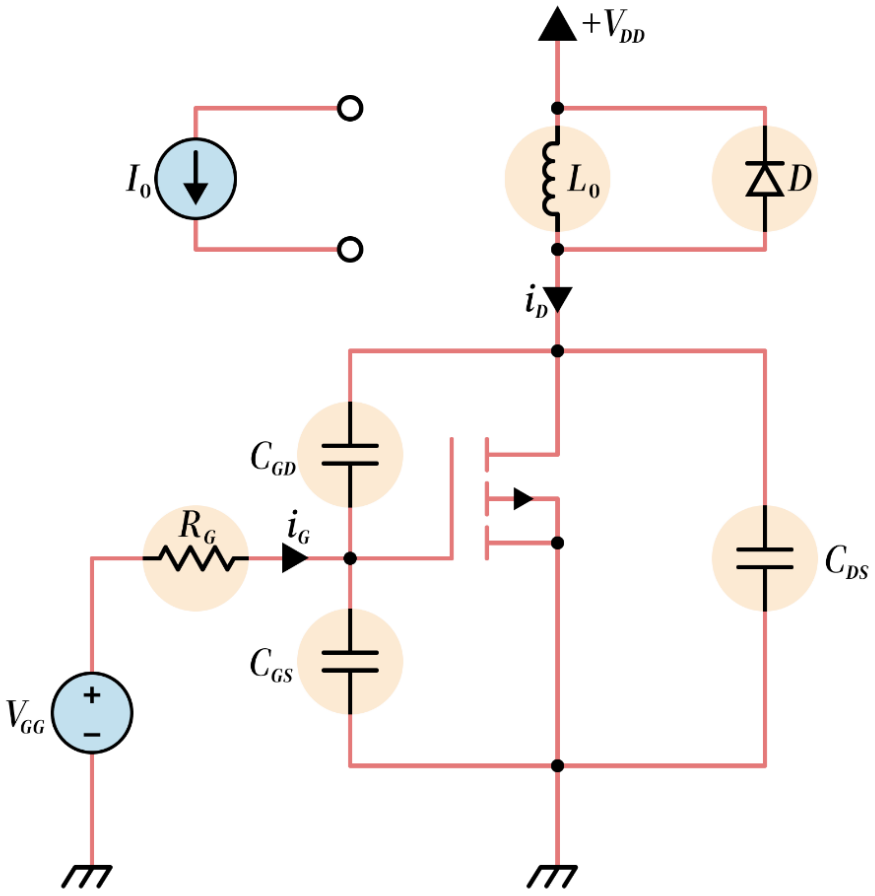


Figure 5b: **Turn-Off MOSFET Waveforms**



As mentioned before, for this Application Note we will consider a simple LSD power electronic circuit under inductive load. We will assume that the load inductance (L_0) is large enough to consider the current through it as constant with value I_o (modeled with a current source in **Figure-6**). Also, a lossless flyback diode D (see **Figure-6**) used to pick up the load current during the MOSFET OFF-state is included.

Figure 6: **LSD Circuit with Inductive Load**

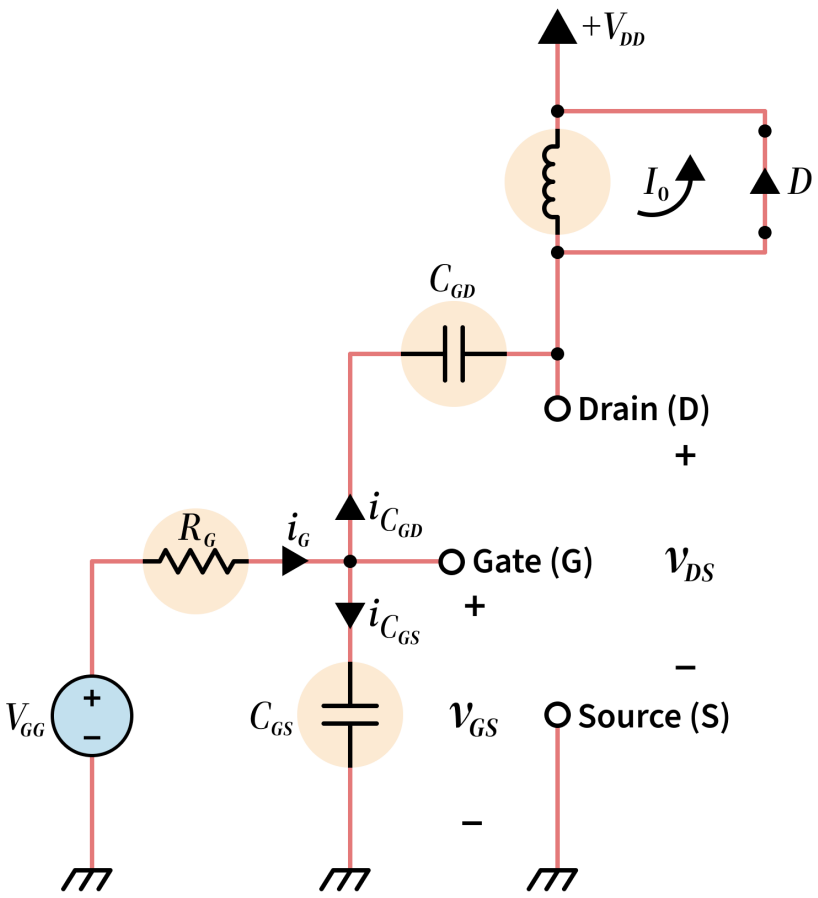


3.1: Turn-On Transition ($t_{10_{ON}}$, $t_{21_{ON}}$, $t_{32_{ON}}$)

3.1.1: t_{ON_10} – Turn-On Delay

First, let's assume the device is off, the load current I_0 flows through D and $v_{GS} = V_{GG} = 0$. The voltage $v_{DS} = V_{DD}$ and $i_G = i_D = 0$. At $t = t_0$, the voltage V_{GG} is applied (**Figure-5a**). The sudden voltage in V_{GG} starts moving charge from C_{GS} and C_{GD} through R_G.

Figure 7: **MOSFET during $t_{10_{ON}}$ with $v_{GS} < V_{th}$ and $i_D = 0$**



During $t_0 \leq t < t_1$ $(t_{10_{ON}})$, $v_{GS} < V_{th}$ having the MOSFET in the cut-off region with $i_D = 0$ regardless of v_{DS} value.

This interval represents the delay turn-on time needed to bring voltages at C_{GS} and C_{GD} from zero to V_{th} and from V_{DD} to $V_{DD} - V_{th}$, respectively. The expression for the $t_{10_{ON}}$ can be obtained considering that the Gate current is given by:

$$i_G = i_{C_{GS}} + i_{C_{GD}}$$	**(1)**

Where:

$$i_{C_{GS}} = C_{GS}\frac{dv_{GS}}{dt}; \quad i_{C_{GD}} = C_{GD}\frac{d(v_{GS} - v_{DS})}{dt}$$

Given that during t_{ON_10} the only voltage changing with time is v_{GS} ($v_{DS} = V_{DD}$, constant) we can rewrite the equation as follows:

$$i_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt}$$

On the other side, $i_G = (V_{GG} - v_{GS})/R_G$, so the equation can be expressed as:

$$\frac{V_{GG} - v_{GS}}{R_G} = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt}$$

Therefore, solving the differential equation for v_{GS}, $t > t_0$ and $v_{GS}(t_0) = 0$ we obtain:

$$v_{GS}(t) = V_{GG}\left(1 - e^{-(t-t_0)/\tau}\right)$$

where τ is defined by

$$\tau = R_G(C_{GS} + C_{GD})$$	**(2)**

This result is valid as long as $v_{GS} < V_{th}$ and $i_D = 0$. Solving for $t_{10_{ON}}$:

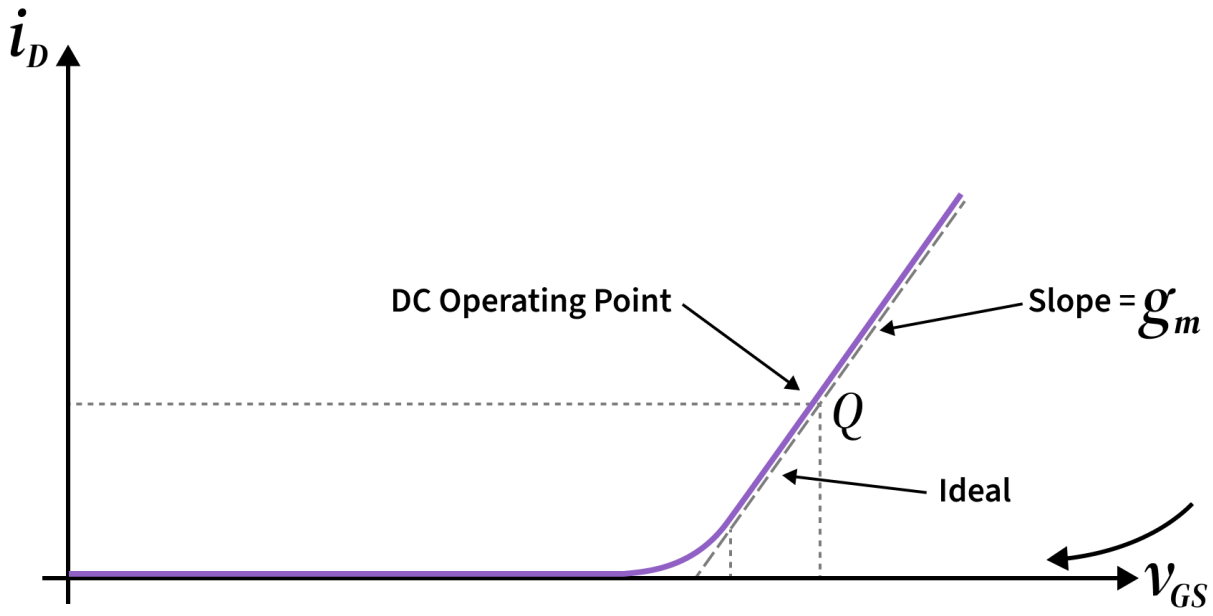
$$t_{10_{ON}} = \tau ln\left(\frac{V_{GG}}{V_{GG} - V_{th}}\right)$$	**(3)**

3.1.2: $t_{21_{ON}}$ – Rise Time

For $t_1 \leq t < t_2$ ($t_{21_{ON}}$) the condition $v_{GS} > V_{th}$ is true causing the MOSFET to start conducting having $i_D \neq 0$. This initial stage of the turn-On current is given by the transconductance equation:

$$i_D = g_m(v_{GS} - V_{th})$$

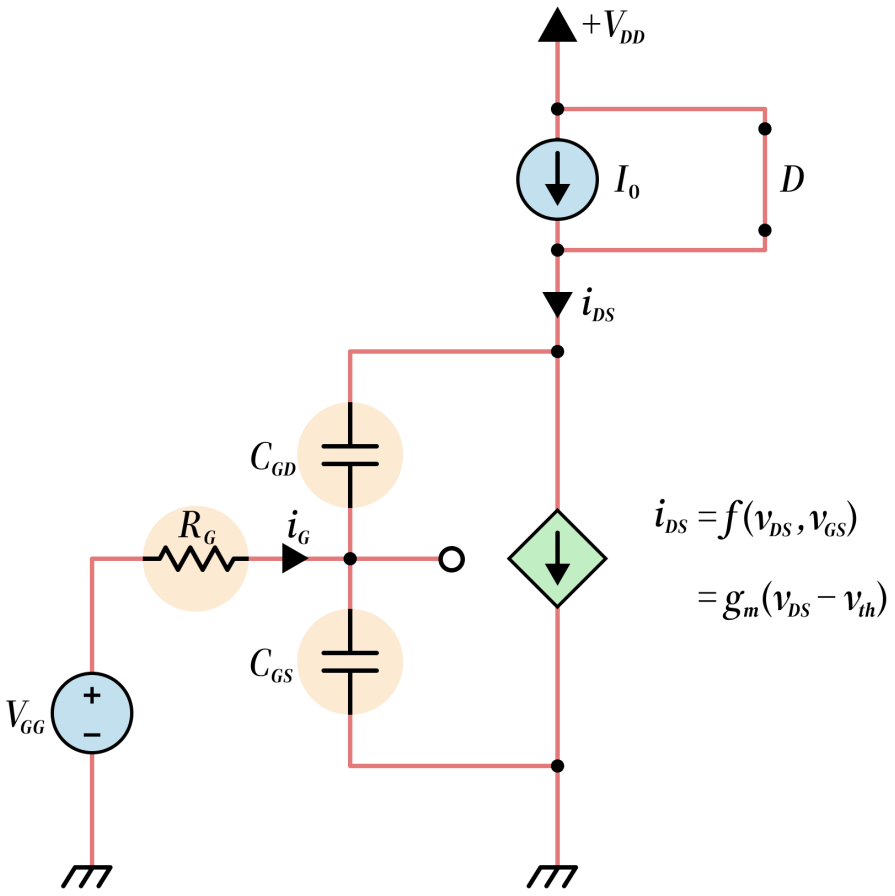
Figure 8: **Input Transfer Characteristics for Small Changes**



As long as $v_{GS} < V_{\text{plateau}}$, the equation for v_{GS} remains the same as in $t_{10_{ON}}$, so:

$$i_D(t) = g_m\left[V_{GG}\left(1 - e^{-(t-t_0)/\tau}\right) - V_{th}\right]$$

Figure 9: **MOSFET during $t_{21_{ON}}$ with $v_{GS} > V_{th}$ and $i_D < I_0$**



Reaching $t = t_2$, i_D arrives at its maximum value of I_0. Considering $i_D(t_2) = I_0$, the time interval $t_2 - t_0$ can be solved from $i_D(t)$ equation previously found, resulting:

$$t_2 - t_0 = -\tau ln\left[\frac{g_m(V_{GG} - V_{th}) - I_0}{g_m V_{GG}}\right] = -\tau ln\left[1 - \frac{1}{V_{GG}}\left(\frac{I_0}{g_m} + V_{th}\right)\right]$$

from **Figure-5a**, when $t = t_2$, v_{GS} is also constant and equal to its On-State Plateau Voltage V_{gp-ON} (S. Liu, et all.), then we can write:

$$i_D(t) = g_m(v_{GS} - V_{th}) \approx I_0 \;\rightarrow v_{GS} = \frac{I_0}{g_m} + V_{th} = V_{gp-ON}$$

allowing to simplify:

$$t_2 - t_0 = -\tau ln\left(1 - \frac{V_{gp-ON}}{V_{GG}}\right) = \tau ln\left(\frac{V_{GG}}{V_{GG} - V_{p-ON}}\right)$$

then finally, $t_{21_{ON}}$ can be obtained using $t_{10_{ON}}$ found previously:

$$t_{21_{ON}} = (t_2 - t_0) - t_{10_{ON}}$$

$$t_{21_{ON}} = \tau ln\left(\frac{V_{GG}}{V_{GG} - V_{p-ON}}\right) - \tau ln\left(\frac{V_{GG}}{V_{GG} - V_{th}}\right)$$

$$t_{21_{ON}} = \tau ln\left(\frac{V_{GG} - V_{th}}{V_{GG} - V_{p-ON}}\right)$$	**(4)**

3.1.3: $t_{32_{ON}}$ – Turn-On Plateau

For $t_2 \leq t < t_3$ ($t_{32_{ON}}$), $i_D = I_0$ and C_{DS} discharges from $v_{DS} = V_{DD}$ to $v_{DS} = I_0 R_{DSon}$, where R_{DSon} is the On-state resistance of the MOSFET.

Since v_{GS} during $t_{32_{ON}}$ is constant, the entire gate current flows through C_{GD}:

$$i_G(t) = i_{C_{GD}}$$

$$i_G(t) = C_{GD}\frac{d(v_{GS} - v_{DS})}{dt}$$

and:

$$i_G(t) = -C_{GD}\frac{dv_{DS}}{dt}$$

$$i_G(t) = \frac{V_{GG} - v_{GS}}{R_G}$$

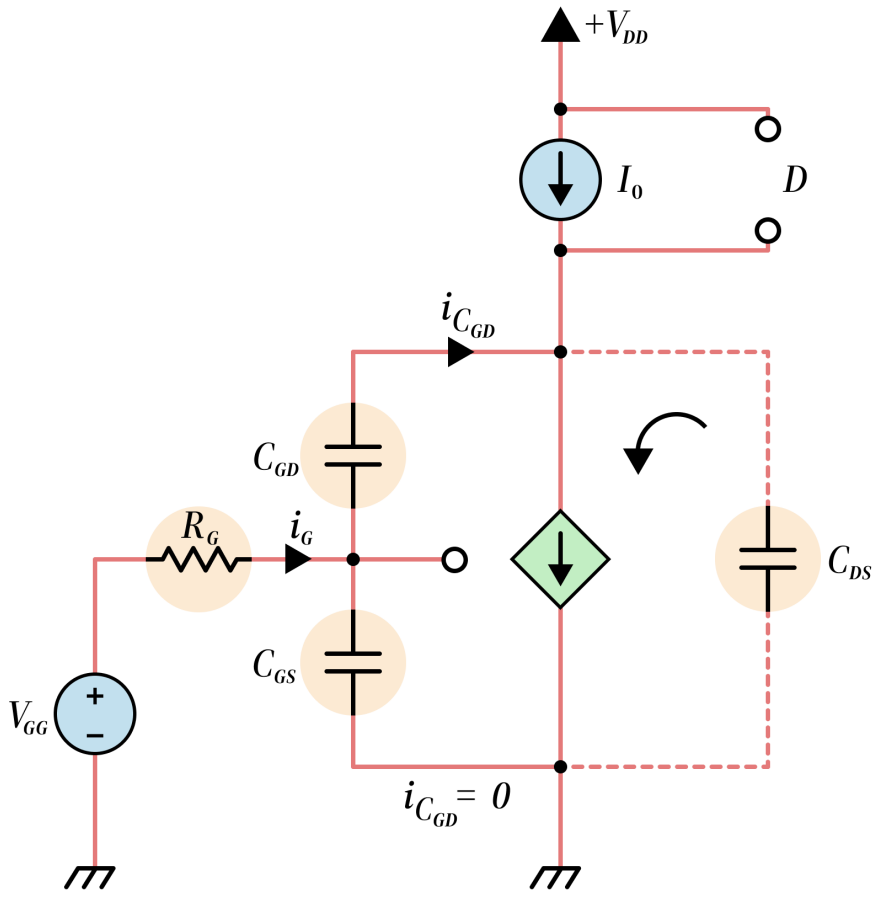
considering $v_{GS} = V_{gp-ON}$, $v_{DS}(t_2) = V_{DD}$ and the interval $\Delta t = t_{32_{ON}}$:

$$\Delta v_{DS} = v_{DS}(t_3) - v_{DS}(t_2) = -\frac{V_{GG} - V_{gp-ON}}{R_G C_{GD}} t_{32_{ON}}$$

The time interval $t_{32_{ON}}$ is determined by assuming that at $t = t_3$ the drain-to-source voltage reaches its minimum value determined by its on resistance:

$$v_{DS}(t_3) \approx I_0 r_{DS(on)}$$

Figure 10: **MOSFET during $t_{32_{ON}}$ with $v_{GS} > V_{th}$, $i_D = I_0$**



Then, the time $t_{32_{ON}}$ is obtained:

$$I_0 r_{DS(on)} - V_{DD} = -\frac{V_{GG} - V_{gp-ON}}{R_G C_{GD}} t_{32_{ON}}$$

$$t_{32_{ON}} = R_G C_{GD} \frac{V_{DD} - I_0 r_{DS(on)}}{V_{GG} - V_{gp-ON}}$$	**(5)**

3.2: Turn-Off Transition ($t_{10_{OFF}}$, $t_{21_{OFF}}$, $t_{32_{OFF}}$)

A similar analysis as the one performed in the previous section can be done for the Turn-Off transition timings. For reason of space, only the results are shown below, but procedure is available upon request.

3.2.1: $t_{10_{OFF}}$ – Turn-Off Delay

Time it takes v_{GS} to go from its maximum value to the plateau value V_{gp-OFF}.

$$t_{10_{OFF}} = \tau \ln \frac{V_{GG}}{V_{gp-OFF}}$$	**(6)**

3.2.2: $t_{21_{OFF}}$ – Turn-Off Plateau

Time it takes v_{DS} to go from its ON-state voltage back to V_{DS_MAX}, in this case $I_0 r_{DS(on)}$ and V_{DD}, respectively:

$$t_{21_{OFF}} = R_G C_{GD} \frac{(V_{DD} - I_0 r_{DS(on)})}{V_p}$$	**(7)**

3.2.3: $t_{32_{OFF}}$ – Fall Time

Time it takes drain current to go from I_{DS_MAX} back to zero:

$$t_{32_{OFF}} = \tau \ln \frac{V_{gp-OFF}}{V_{th}}$$	**(8)**

4: Conclusions and Series Outlook

This Application Note introduced the methodology for calculating switching times, turn-on and turn-off transitions, of Power MOSFETs in low-side driver configurations with inductive loads. These calculations form the foundation for estimating switching losses and comparing device performance.

Upcoming notes in this series will build on this foundation, guiding engineers through the process of extracting key datasheet parameters, performing complete power consumption calculations, and applying the methodology to real MCC MOSFET part numbers. Each note is designed to provide practical insights and tools for making informed component selections in power-sensitive designs.

By using a consistent application example throughout, an LSD circuit with an inductive load, this series aims to simplify the comparison of switching losses across different MOSFETs, whether from multiple vendors or within a single product line.

Bibliography

- Liu, S., Song, S., Xie, N., Chen, H., Wu, X., & Zhao, M. (2021). Miller Plateau Corrected with Displacement Currents and Its Use in Analyzing the Switching Process and Switching Loss. Electronics, 10(16), 2013. https://doi.org/10.3390/electronics10162013

- How to Reduce Power Consumption in a Circuit. (2020, December 18th). https://resources.pcb.cadence.com/blog/2020-how-to-reduce-power-consumption-in-a-circuit

- Elsevier. (n. d.). Power efficient. Science Direct. https://www.sciencedirect.com/topics/computer-science/power-efficient

- Baliga, B. J. (2010). *Advanced Power MOSFET Concepts*. Springer Science & Business Media.