

Beyond R_{thJA} : How to Accurately Predict Junction Temperature Using Electro-Thermal Models

A Practical Guide to Transient Thermal Impedance, Foster and Cauer Models, and SPICE-Based Thermal Simulation

ABSTRACT

In hardware design, thermal modeling is as important as electrical and layout design. While steady-state thermal resistance provides a useful indication of device thermal performance, it does not fully describe the transient thermal response of semiconductor devices. During startup, switching, overload, or repetitive power pulses, junction temperature can change rapidly and may exceed safe operating limits, potentially resulting in device failure and damage to surrounding components.

This application note provides a practical approach to developing electro-thermal models without requiring designers to reproduce the underlying thermal characterization process. Foster and Cauer RC network synthesis are used to generate equivalent thermal models from transient thermal impedance data. The Foster model is used to obtain an equivalent RC representation of the measured thermal response, while the Cauer model provides a thermal network that can be combined with external thermal elements such as heatsinks and thermal interface materials.

The results demonstrate close agreement between the extracted thermal models and the measured steady-state junction temperatures. This validates the modeling methodology and demonstrates how the approach can be extended to simulate other transient thermal conditions.

Keywords: MOSFET, Thermal, Transient, Electronics, Design, Cauer, Foster.

You've selected the right MOSFET, calculated the power dissipation, and verified the steady-state thermal resistance. Yet your prototype still overheats during startup, switching events, or repetitive power pulses. Why? Steady-state thermal resistance parameters such as R_{thJA} cannot fully capture transient thermal behavior, where junction temperature changes dynamically over time. This application note explains how electro-thermal models derived from transient thermal impedance enable accurate junction temperature prediction in SPICE simulations, helping engineers evaluate device performance under real operating conditions.

1. INTRODUCTION

Thermal management is a critical aspect of power semiconductor design, directly affecting device performance, efficiency, and long-term reliability. To support thermal analysis, MCC characterizes thermal performance of its semiconductor devices through laboratory measurements and provides thermal resistance parameters in its datasheets. These steady-state thermal resistance values, such as junction-to-ambient (R_{thJA}) and junction-to-case (R_{thJC}), are widely used to estimate junction temperature under continuous operating conditions.

However, many real-world applications operate under dynamic conditions where devices experience transient power pulses during startup, switching events, overloads, or fault conditions. Under these circumstances, steady-state thermal resistance alone cannot accurately represent the device's thermal response, as junction temperature changes continuously with both power dissipation and time.

To evaluate these transient thermal effects, designers require electro-thermal models derived from transient thermal impedance characteristics. These models enable accurate thermal simulation in SPICE-based tools, allowing engineers to predict junction

temperature, assess repetitive pulse capability, and determine whether a device has sufficient time to cool between power pulses.

This application note explains how MCC develops electro-thermal simulation models from transient thermal impedance data and demonstrates how these models can be implemented in SPICE simulations to improve thermal analysis and support more reliable power electronic designs.

2. HEAT TRANSFER MECHANISMS

Before an electro-thermal model can accurately predict junction temperature, it is important to understand how heat is generated and dissipated within a semiconductor device. Every thermal resistance used in a simulation represents a physical path through which heat travels, from the silicon junction through the package and PCB, and ultimately into the surrounding environment. In power semiconductor devices, electrical losses are converted into heat at the silicon junction. If this heat is not efficiently removed, the junction temperature rises, potentially affecting device performance, efficiency, and long-term reliability. Heat is transferred through three fundamental mechanisms: **conduction**, **convection**, and **radiation**, as illustrated in Figure 1. While all three contribute to heat dissipation, conduction is the dominant mechanism inside semiconductor devices and forms the basis of electro-thermal modeling.

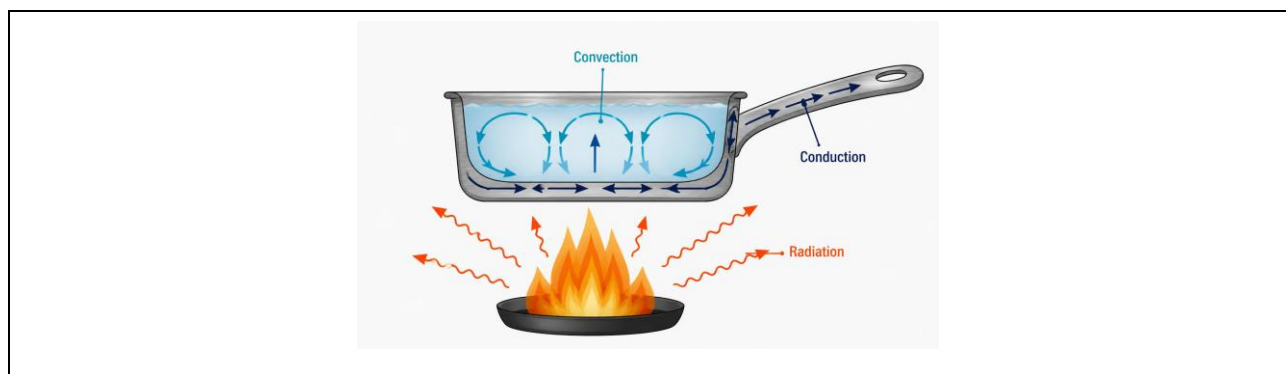


Figure 1: Heat transfer mechanisms

2.1 Conduction

Heat generated at the semiconductor junction is transferred mainly by **conduction** through solid materials. Within the package, it flows from the silicon die through the die-attach material, lead frame or copper clip, solder joints, and package materials to the PCB or an external heatsink. Because conduction governs the movement of heat within the semiconductor package, it forms the basis of the thermal resistance network used in electro-thermal modeling.

2.2 Convection

After heat leaves the semiconductor package, it travels through the applicable thermal path, which may include the PCB, thermal interface materials, and heatsink before being dissipated to the surrounding environment. This stage of heat removal occurs primarily through **convection**, where heat is transferred from the surface of the PCB or heatsink to the surrounding air. Cooling performance depends on factors such as airflow, heatsink geometry, PCB copper area, and ambient temperature.

2.3 Radiation

Although **radiation** also contributes to heat dissipation, its effect is typically much smaller than conduction and convection in power semiconductor applications. Consequently, semiconductor thermal models focus primarily on the conductive heat path from the junction to the package, PCB, and heatsink. This is why electro-thermal models represent the device using equivalent thermal resistance-capacitance (RC) networks. Each thermal resistance corresponds to a section of the conductive heat path, while each thermal capacitance represents the ability of a material to store heat. Together, these elements reproduce how junction temperature changes over time under transient power dissipation and provide the foundation for SPICE-based electro-thermal simulation.

3. FROM HEAT FLOW TO THE THERMAL MODEL

Understanding heat flow through a semiconductor device is only the first step in thermal analysis. To predict junction temperature under real operating conditions, this physical behavior must be converted into a mathematical model for simulation.

Electro-thermal modeling achieves this by representing the thermal behavior of a semiconductor device using an equivalent electrical circuit. Similar to how electrical circuits describe the flow of current through resistors and capacitors, thermal networks describe the flow of heat through thermal resistances and thermal capacitances. This analogy enables thermal behavior to be analyzed using standard SPICE-based circuit simulators.

Before introducing the electro-thermal analogy, it is useful to examine how heat travels through a semiconductor package and how this physical heat flow is represented as a thermal resistance network.

3.1 From Physical Heat flow to a Thermal Resistance Network

Heat is generated at the semiconductor junction, where electrical power is dissipated within the silicon die. From the junction, heat flows through the internal package structure before reaching the PCB, heatsink, and ultimately the surrounding environment.

For most semiconductor packages, heat is transferred primarily through the bottom of the package. The thermal path includes the silicon die, die attach material, lead frame or copper clip, solder joints, PCB copper, thermal vias (when present), thermal interface materials (TIM), heatsinks, and finally the surrounding air.

Within the semiconductor package, heat is transferred primarily by conduction because the internal materials form a continuous physical thermal path. Under steady-state conditions, this conductive path can be represented by the junction-to-case thermal resistance (R_{thJC}).

However, advanced package technologies can provide additional thermal paths to improve heat dissipation. Figure 2 illustrates the thermal conduction paths of MCC's **MCACLS290N04YHE3** Dual-Side Cooling (DSC) Power MOSFET. Unlike conventional packages that dissipate heat mainly through the PCB, the Dual-Side Cooling package provides an additional conductive path through the exposed top copper surface, reducing overall thermal resistance and improving cooling performance in high-power applications.

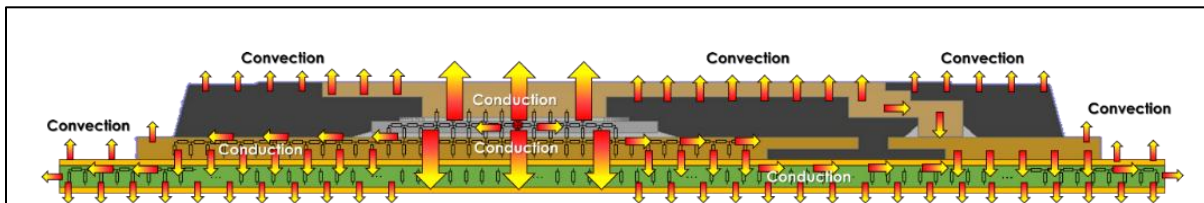


Figure 2: Heat flow through a MCC Dual-Side Cooling Power MOSFET

While Figure 2 illustrates the physical movement of heat through the semiconductor package, thermal analysis requires this heat flow to be represented mathematically. Figure 3 simplifies the physical structure into a thermal resistance network, where each section of the heat flow path is modeled by an equivalent thermal resistance.

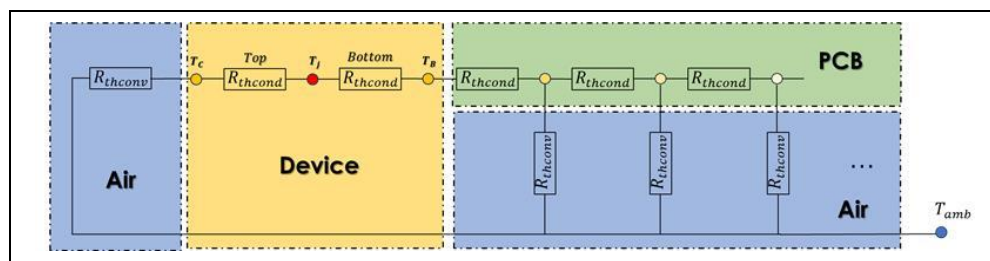


Figure 3: Thermal resistance model

The Device block represents the internal thermal resistance of the semiconductor package, while the **PCB** and **Air** (Convection) blocks represent the external thermal path through the PCB, thermal interface materials, heatsinks, and surrounding environment. This equivalent representation provides the foundation for electro-thermal modeling and transient thermal simulation.

For conventional semiconductor packages, heat transfer through the top of the package is typically limited by the thermal resistance of the mold compound. As a result, datasheets commonly specify a primary thermal path through the bottom of the package ($R_{thJC(Bot)}$). However, packages such as the [MCACLS290N04YHE3](#) Dual-Side Cooling package shown in Figure 2, incorporate a copper heat-spreading path connected directly to the die, creating an additional low-resistance thermal path through the top of the package ($R_{thJC(Top)}$). As a result, heat can be dissipated through both the top and bottom surfaces, and separate transient thermal resistance characteristics are provided for the two paths.

3.2 Understanding Thermal Resistance

Thermal resistance quantifies how effectively heat can be transferred from one point to another. Similar to electrical resistance, higher thermal resistance restricts the flow of heat, resulting in a greater temperature rise for a given power dissipation.

Thermal resistance depends on the thermal conductivity and physical dimensions of the material. Thermal conductivity, represented by k , describes how effectively a material conducts heat. Materials with higher thermal conductivity, such as silver, copper, and gold, transfer heat more efficiently, while materials with lower thermal conductivity, such as FR-4 and air, provide greater resistance to heat flow. Table 1 shows the thermal conductivity constant for common materials involved in electronics applications.

Table 1: Thermal conductivity of various materials (Thermtest Instruments, n.d.)

Material	K in units of $\frac{W}{m \cdot K}$
Silver	426.77
Copper	397,48
Gold	317.98
Silicon	125.52
Solder (SnPb)	50.208
Water	0.60652
FR4	0.3
Air	0.023

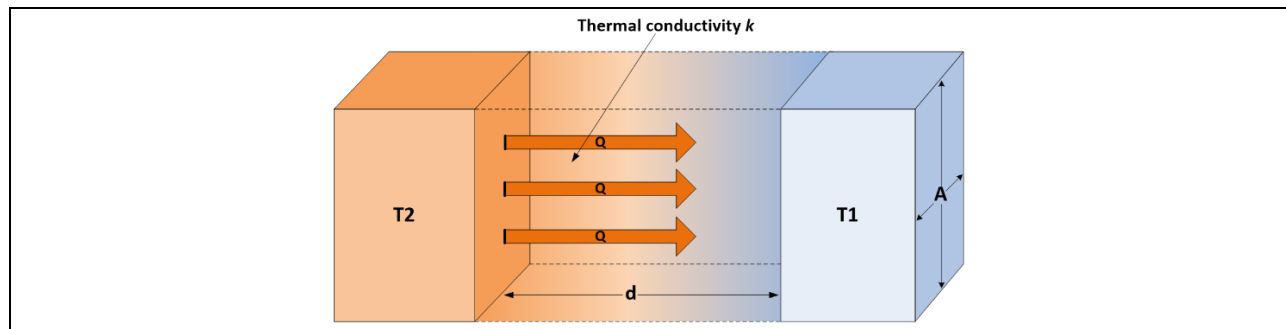


Figure 4: Thermal conductivity schematic - Heat transfers from a hotter object to a colder object

In Figure 4, T2 represents the hotter side and acts as the thermal source, while T1 represents the cooler side and acts as the thermal sink. The temperature difference is therefore:

$$\Delta T = T_2 - T_1 \quad (\text{Eq. 1})$$

Finally, the geometry of the device will play a role because shorter distances and larger areas will transfer heat easily than longer distances and smaller areas leading to:

$$\frac{Q}{t} = \frac{kA\Delta T}{d} \quad (\text{Eq. 2})$$

Where:

$Q \rightarrow$ Heat flow transferred

$t \rightarrow$ Time

$A \rightarrow$ Cross sectional area of the material

$\Delta T = T_{hot} - T_{cold} \rightarrow$ Difference in temperature between one side of the material and the other

$d \rightarrow$ Thickness of the material

$k \rightarrow$ Thermal conductivity constant $\rightarrow$ Larger for materials that transfer heat well, smaller for materials that transfer heat poorly.

From previous equation, solving for ΔT , we have:

$$\Delta T = \left(\frac{Q}{t}\right) \left(\frac{d}{kA}\right) \quad (\text{Eq. 3})$$

Finally, taking Eq. 3, we can define the device Thermal Resistance as:

$$R_{\theta} = \frac{\text{Thickness of the material } d}{\text{Thermal conductivity } k * \text{Cross sectional area } A} \quad (\text{Eq. 4})$$

and knowing that Power dissipation can be written as:

$$P_{Loss} = \frac{\text{Heat flowing through semiconductor (energy) } Q}{\text{Time } t} \quad (\text{Eq. 5})$$

The thermal resistance can be expressed as a “Ohm’s Law” form equation which is the basis for the electro-thermal analogy of the following section:

$$R_{\theta} = \frac{\text{Temperature difference } \Delta T}{\text{Thermal Power dissipation } P_{Loss}} \quad (\text{Eq. 6})$$

3.3 Electro-Thermal Analogy

In previous section a “Thermal Ohm’s Law” was developed. This idea allows us to do a mapping between thermal/heat movement factors and electrical charge movement factors, i.e. an electro-thermal analogy that lets us do typical calculations performed in electrical circuits using thermal variables.

Electrical systems are described by:

$$V = IR \quad (\text{Eq. 7})$$

Similarly, thermal systems can be described by:

$$\Delta T = P \times R_{\theta} \quad (\text{Eq. 8})$$

Having the “Thermal Ohm’s law” is sufficient to perform steady-state calculations using resistive voltage divider circuits as a basis for analysis. However, in this document we want to find a way of having a transient thermal analysis. With that, we will, intuitively map an electrical capacitance with a “thermal capacitance” which is, more formally, known as heat capacity. Therefore, just as a capacitor takes time to charge, a mass will take time to heat up. Such capacitance is simply the amount of heat required to raise the temperature of the object by 1K [J/K].

Using the described analogy, a current source in a circuit will describe a power source in the thermal sense. Ambient and Junction temperatures will be represented through node voltages and so on. Table 2 shows electro-thermal analogy mapping, including physical units.

Table 2: Thermal analogy

Electrical	Thermal
Potential Difference, V (V)	Temperature Difference, ΔT (K)
Resistance, R (Ω)	Thermal Resistance, R_{th} (K/W)
Current, I (A)	Heat Flow Rate, P (W)
Capacitance, C (F)	Thermal Capacitance, C_{th} (J/K)

4. ELECTRO-THERMAL MODEL

The electro-thermal analogy introduced in the previous chapter provides the foundation for modeling the thermal behavior of semiconductor devices using equivalent electrical circuits. By representing thermal resistances and thermal capacitances as electrical components, both steady-state and transient junction temperature can be analyzed using SPICE-based simulation tools.

4.1. Steady-State Model

Using the electro-thermal analogy described in the previous chapter, steady-state thermal behavior can be analyzed using a simple resistive network. Similar to a voltage divider in an electrical circuit, the thermal network consists of a series of thermal resistances that determine the temperature rise from ambient to the semiconductor junction.

Consider a device dissipating **6 W** of power, modeled as a **6 A** current source in the equivalent thermal circuit. The voltage at the junction node represents the junction temperature (**T_J**). The thermal network consists of the junction-to-case thermal resistance (**R_{thJC}**), thermal-via resistance (**R_{thv}**), thermal interface material resistance (**R_{thTIM}**), and heatsink thermal resistance (**R_{thHS}**).

Applying the equivalent resistive network calculation gives a junction temperature of **T_J = 103°C** when the ambient temperature is **T_A = 25°C**, as illustrated in Figure 5.

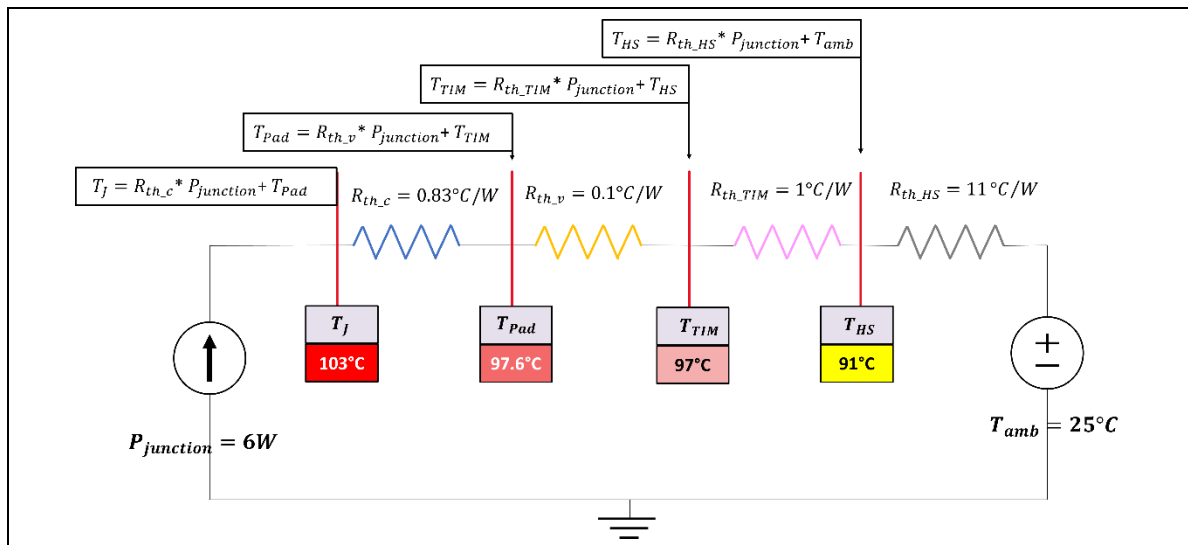


Figure 5. Steady-state calculation

4.2 Transient model using Foster Thermal Model

The transient thermal impedance curve provided in a semiconductor datasheet can be used to develop a thermal model for simulating the device response to single and repetitive power pulses.

Based on the electro-thermal analogy introduced in Chapter 3, the thermal behavior of the device can be represented by an equivalent thermal circuit whose transient response matches the datasheet's thermal impedance curve. This process, known as circuit synthesis, is widely used in electrical engineering to develop equivalent circuit models for applications such as filter design and control systems.

One approach is the Foster thermal model, which represents the device using multiple parallel resistor-capacitor (RC) branches. The transient response of this network is well established in electrical circuit theory and can be expressed as:

$$Z_{th}(t) = \sum_{i=1}^n R_i \left(1 - e^{-\frac{t}{\tau_i}} \right), \text{ where } \tau_i = R_i C_i \quad (Eq.9)$$

To obtain the Foster model, data points are extracted from the transient thermal impedance curve, as shown in Figure 6. Typically, one data point per decade of pulse duration is sufficient. The extracted data can then be fitted to the Foster model using an appropriate numerical method to determine the R_i and C_i values for the required number of RC branches. In most cases, four to five RC branches are sufficient to accurately represent the thermal behavior of a semiconductor device.

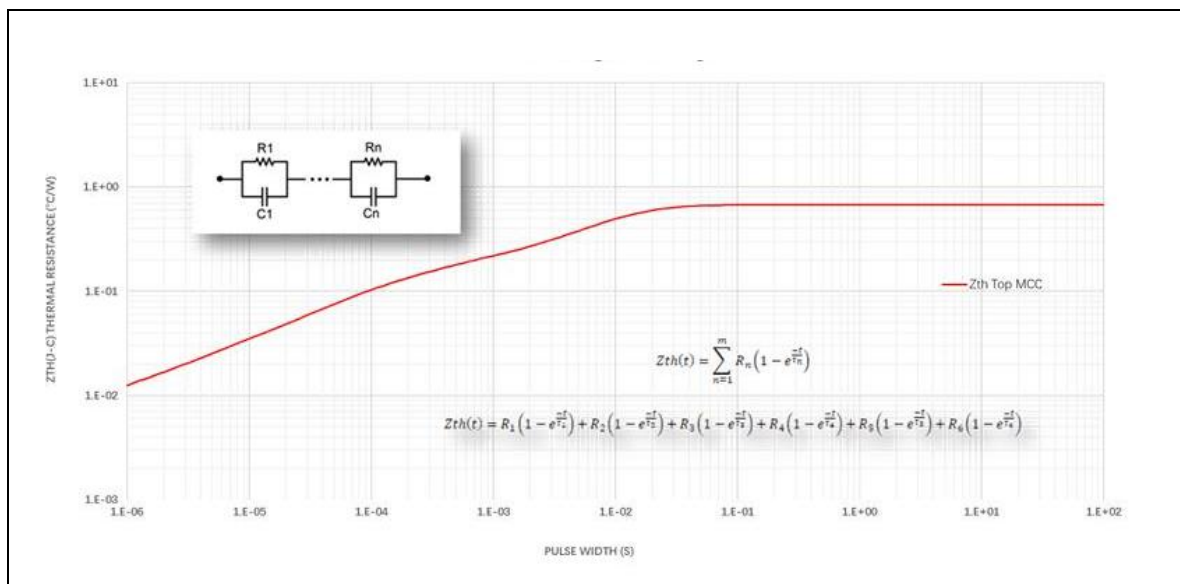


Figure 6: Thermal impedance of a component

It is important to note that the R_i and C_i elements in a Foster model do not represent specific physical locations within the device. Instead, the model is a mathematical representation used to reproduce the thermal behavior between its terminals, in this case, the junction and case in a black-box manner.

The Foster model is relatively easy to extract from transient thermal impedance data. However, it may become unstable or produce inaccurate results when connected to other thermal models within the application, such as an external heatsink. This limitation is significant when the thermal model needs to be combined with the surrounding thermal environment.

4.3 Transient model using Cauer Thermal Model

The Cauer model provides an alternative thermal model with a more direct physical interpretation and greater stability during simulation. It is formed as a ladder network, with resistors connected in series and capacitors connected from each node to ground, as shown in Figure 7.

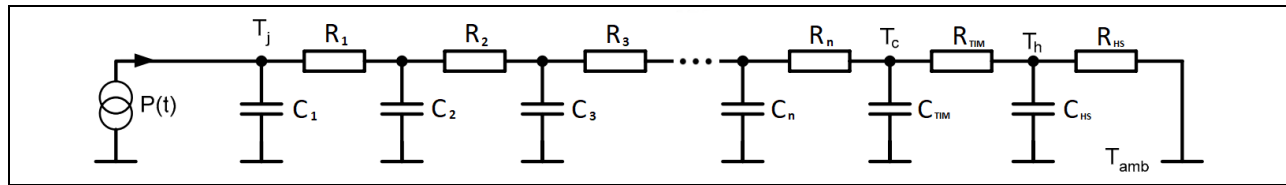


Figure 7: Cauer Model RC network schematic

The Cauer model also allows external thermal elements to be connected more naturally to the device model. Heatsinks, thermal vias, thermal interface materials, and other thermal networks can therefore be incorporated into the simulation. This enables the complete thermal path to be modeled and can improve the accuracy of junction temperature prediction.

Unlike the Foster model, the internal nodes of a Cauer model can have physical meaning and may represent different sections of the device's thermal path when the corresponding physical information is available.

However, the coefficients of the Cauer ladder network are not as straightforward to extract as those of the Foster model. Therefore, the Cauer model coefficients are obtained by first determining the Foster model coefficients.

The Cauer coefficients are then obtained by mathematically transforming the Foster model into an equivalent Cauer network with the same number of RC elements, as described in 4.2. The Cauer model is defined in JEDEC's Standard JESD No.51-14 (*Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat Flow Through a Single Path*, 2010) as:

$$Z_{th}(s) = \frac{1}{Y_1(s) + \frac{1}{Z_1(s) + \frac{1}{Y_2(s) + \dots + \frac{1}{Z_n(s)}}}} \quad (Eq. 10)$$

Unlike the Foster model, the Cauer model equation is expressed in the frequency domain, $Z_i(s) = R_i$ and $Y_i(s) = sC_i$, where $s = j\omega$. It is also important to note that $Z_0(s)$ must be equal to zero for the ladder network to remain valid. The relationship between the equation coefficients and the corresponding ladder network elements is illustrated in Figure 8.

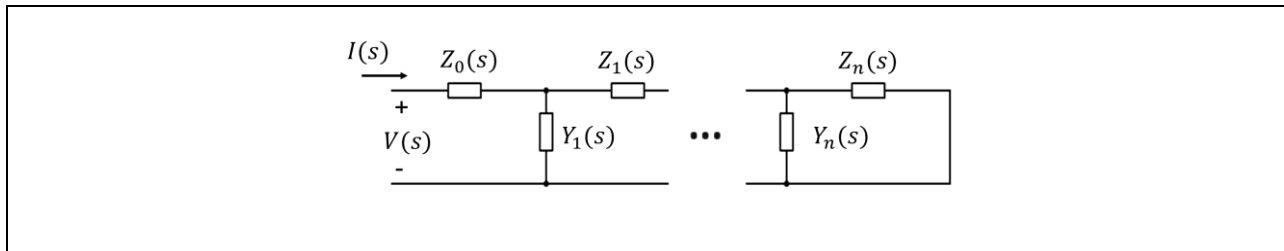


Figure 8: Cauer schematic representing Cauer Model definition

5. TESTING AND THERMAL SIMULATIONS

5.1 Testing Conditions

To validate the performance of the thermal model extraction method, two MCC power MOSFETs were tested: [MCACL330N04Y](#), housed in the DFN5060-C package and referred to as **DFN** hereafter; and [MCACLS330N04YAHE](#), housed in the DFN5060-DSC package and referred to as **DSC**. Both devices were tested under the conditions specified in Table 3.

The test was conducted for 3 hours using the PCB shown in Figure 9. The PCB was made of standard FR-4, double-sided, with 1 oz. of copper. The heatsinks shown in Figure 10 were made of aluminum and measured 50 mm × 50 mm × 14 mm. For DFN, the heatsink was

mounted to the bottom of the PCB. For DSC, the heatsink was placed in contact with the top cooling pad, while the bottom of the PCB remained exposed to air.

Table 3: Test conditions and thermal resistance in laboratory measurements and simulation.

Test Condition	Units	MCACL330N04Y (DFN)	MCACLS330N04YAHE3 (DSC)
Heat Current 15A $T_A = 25^\circ\text{C}$	VSD (Body-Diode voltage) (V)	0.511	0.542
	T_j ($^\circ\text{C}$)	165.1	143.9
	P_d (W)	7.665	8.13
	R_{thj-a} ($^\circ\text{C}/\text{W}$)	18.9	15.2
	Package	DFN5060-C	DFN5060-DSC

At the end of the test, the steady-state junction temperature was measured for each device. The final junction temperature was 165.1°C for DFN and 143.9°C for DSC. The power dissipated at the junction was $P_{D_{DFN}} = 0.5V(15A) = 7.665W$ for DFN and $P_{D_{DSC}} = 0.542V(15A) = 8.13W$ for DSC.

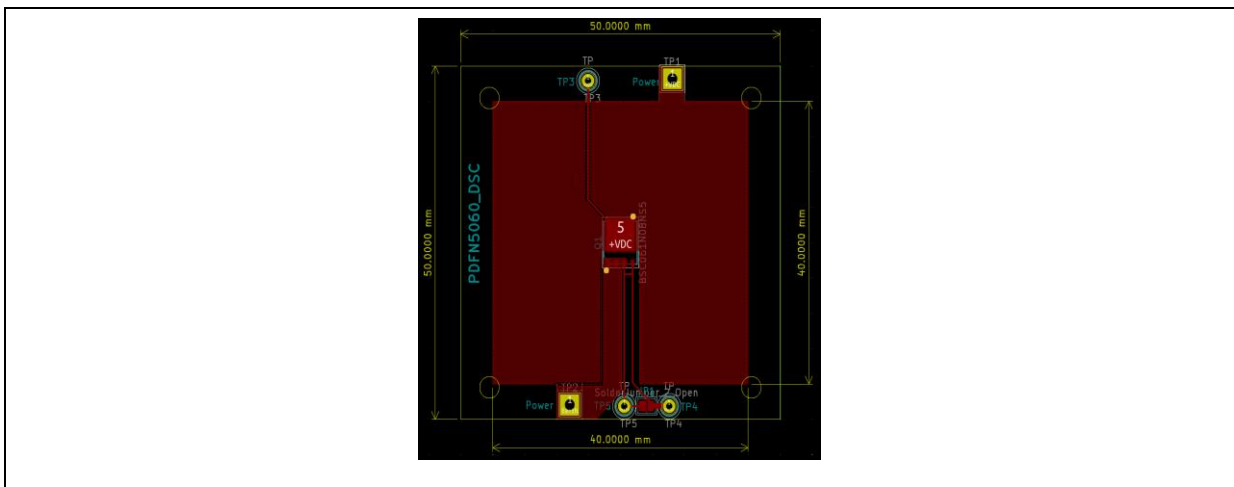


Figure 9: PCB layout for the test

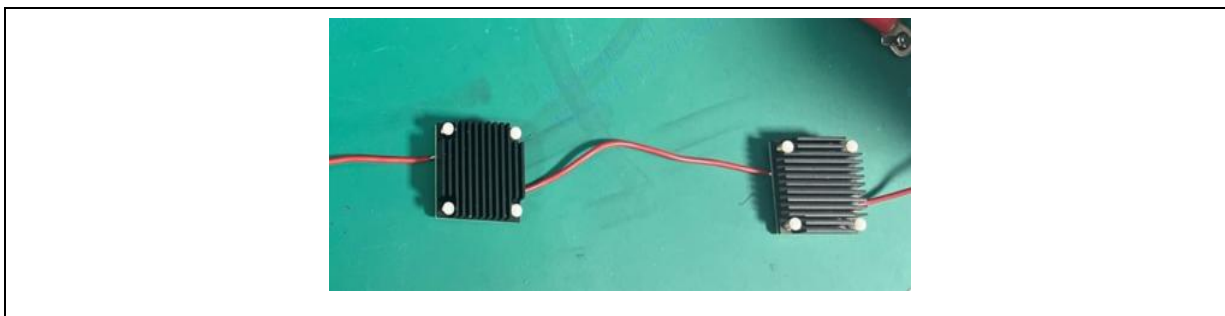


Figure 10: Implementation MCACL330N04Y and MCACLS330N04YAHE3 with heatsinks

5.2 Thermal Models for DUTs

By applying the techniques described in Chapter 3 of this document, the thermal models for each of the components in Table 4 and 5 were obtained.

Table 4: Cauer model from DSC component

Cauer Models		
	(Lumped Elements) Top	(Lumped Elements) Bottom
R1	0.0277308 °C/W	0.021001074 °C/W
R2	0.1421131 °C/W	0.089937513 °C/W
R3	0.0578536 °C/W	0.082698100 °C/W
R4	0.3683493 °C/W	0.143751045 °C/W
R5	0.0686746 °C/W	0.006709425 °C/W
R6	0.0124484 °C/W	0.010002800 °C/W
C1	0.0000606864 J/K	0.0000787109 J/K
C2	0.0008489300 J/K	0.0008196120 J/K
C3	0.0092995900 J/K	0.0051714144 J/K
C4	0.0091127071 J/K	0.0057819959 J/K
C5	0.0836668200 J/K	0.5013800000 J/K
C6	4.3228013700 J/K	2.3618634400 J/K

Table 5. Cauer model from DFN component

	(Lumped Elements) Bottom
R1	0.02675820 °C/W
R2	0.01006201 °C/W
R3	0.10830350 °C/W
R4	0.54734510 °C/W
R5	0.10635110 °C/W
R6	0.00117993 °C/W
C1	0.00003667 J/K
C2	0.00060927 J/K
C3	0.00130847 J/K
C4	0.01806036 J/K
C5	0.01940538 J/K
C6	3.062367401 J/K

5.3 Simulation results

Based on the conditions in Table 3, the simulation shown in Figure 11 uses power sources with magnitudes matching the power dissipated by each component during the bench measurements. Following the electro-thermal analogy described previously, these power sources are represented as current sources and are connected to the $T_{j(DFN)}$ and $T_{j(DSC)}$ nodes, which represent the junction temperatures of the respective components.

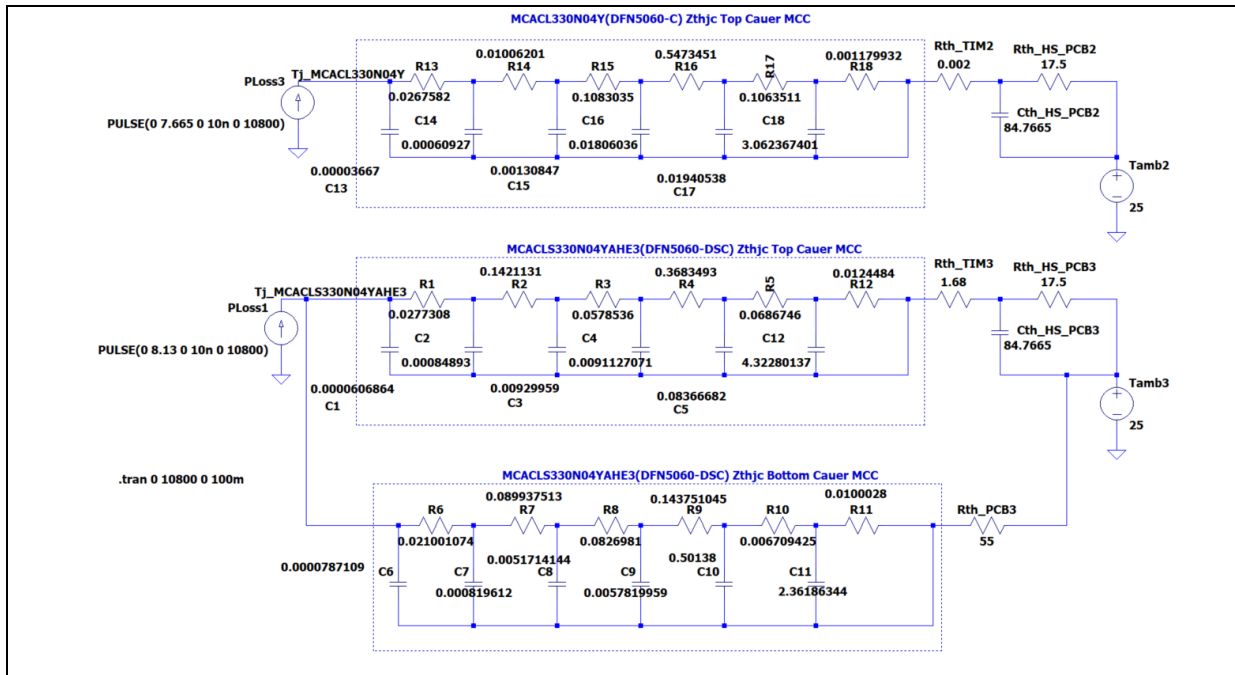


Figure 11: Cauer models for DFN and DSC parts in LTspice® simulator

In addition, the heatsink is represented by a thermal resistance of $R_{th_HS_PCB2} = 17.5\text{ }^{\circ}\text{C/W}$ and a thermal capacitance of $C_{th_HS_PCB2} = 84.7665\text{ J/K}$, also adding the thermal interface material resistance with a resistor of $R_{th_TIM2} = 0.002\text{ }^{\circ}\text{C/W}$ for the MCACL330N04Y and $R_{th_TIM3} = 1.68\text{ }^{\circ}\text{C/W}$ for the MCACLS330N04YAHE3 with an ambient temperature of $T_{amb2} = T_{amb3} = 25^{\circ}\text{C}$ connected to the terminal node. The resulting thermal network is shown in Figure 11. For the DSC, the bottom side of the PCB was exposed to air during testing, thus the thermal resistance of the FR-4 PCB was modeled as $R_{th_PCB3} = 55^{\circ}\text{C/W}$.

It is seen in Figure 12 that after 10800 seconds or 3 hours of simulation time the final simulated temperatures were $T_{jDFN} = 165.1924^{\circ}\text{C}$ and $T_{jDSC} = 143.8084^{\circ}\text{C}$. These results match closely with the steady-state temperatures measured during the bench test: 165.1°C for DFN and 143.9°C for DSC.

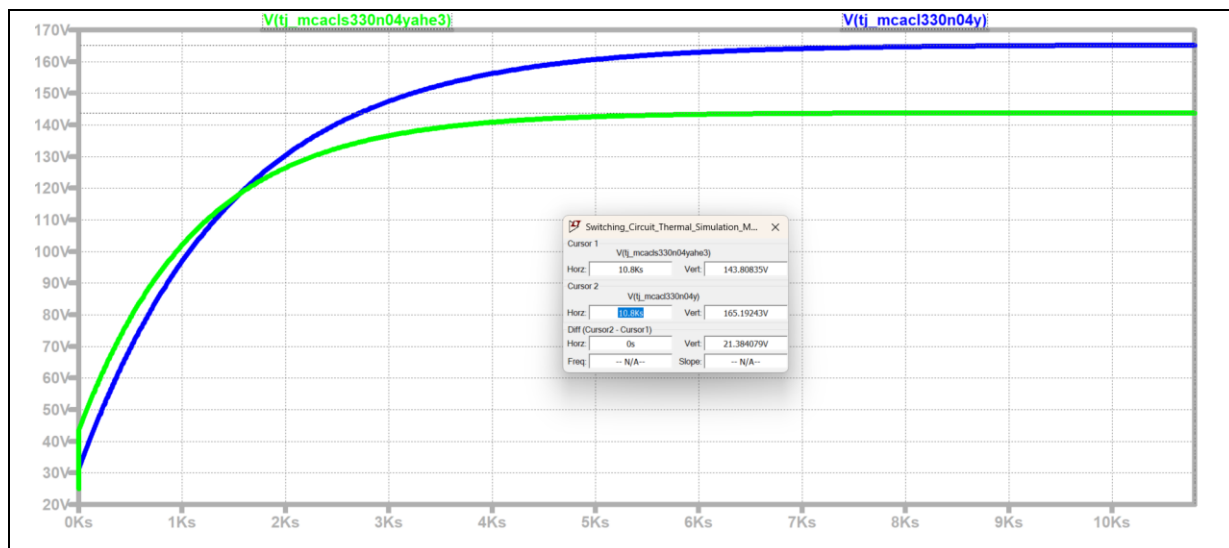


Figure 12: Simulation of MCACLS330N04Y and MCACLS330N04YAHE3 Cauer model under test conditions from Table 3

The close agreement between the simulated and measured junction temperatures demonstrates that the extracted thermal models accurately represent the steady-state thermal behavior of both devices under the specified test conditions.

6. SIMULTANEOUS ELECTRICAL AND THERMAL SIMULATION IN SPICE

6.1 Integrated Model with Electrical and Thermal Behaviors

The simulation presented in Chapter 5 is a thermal-only simulation based on the electro-thermal analogy described in Chapter 3. In other words, it does not include the electrical behavior of the device; instead, it uses a fixed, predefined power pulse as the thermal input.

A SPICE-based simulator can extend this approach by simulating electrical and thermal behaviors simultaneously. The thermal model can be embedded within the electrical SPICE model as a SPICE netlist, with a terminal connected to the device's junction thermal node. This allows the dissipated power to be updated dynamically based on the electrical

simulation, while the resulting junction temperature is returned as a node voltage at the junction terminal of the device SPICE model.

Figure 13 presents a netlist of an electrical model of the MCC [MCACLS330N04YAHE3](#) Power MOSFET with an embedded thermal model. The model incorporates two additional terminals: T_j , which represents the junction temperature, and T_c , which represents the case temperature. To prevent numerical convergence errors during simulation, the T_c terminal must be connected either to ground or to a reference source, typically one representing the ambient temperature.

```
.SUBCKT MCACLS330N04YAHE3_PS D G S Tj Tct Tcb

* Tct is case for Top
* Tcb is case for Bottom

Vd D D1 0 Rser=0 Cpar=0
G2 0 Tj value={v(D, S)*i(Vd)}

* Cuaer thermal model for Dual side cooling

* Top side
R1T Tj 1 0.0277308
R2T 1 2 0.1421131
R3T 2 3 0.0578536
R4T 3 4 0.3683493
R5T 4 5 0.0686746
R6T 5 Tct 0.0124484

C1T Tj Tct 0.0000606864
C2T 1 Tct 0.00084893
C3T 2 Tct 0.00929959
C4T 3 Tct 0.0091127071
C5T 4 Tct 0.08366682
C6T 5 Tct 4.32280137

* Bottom Side
R1B Tj 6 0.021001074
R2B 6 7 0.089937513
R3B cc7 8 0.0826981
R4B 8 9 0.143751045
R5B 9 10 0.006709425
R6B 10 Tcb 0.0100028
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Figure 13: SPICE netlist of the thermal model for the MCACLS330N04YAHE3

Figure 14 shows an example of integrated electrical and thermal simulation. Unlike the simulation described in Chapter 5, the power injected into the device is no longer represented by a fixed current source. Instead, the power is modeled using a behavioral current source embedded within the SPICE model.

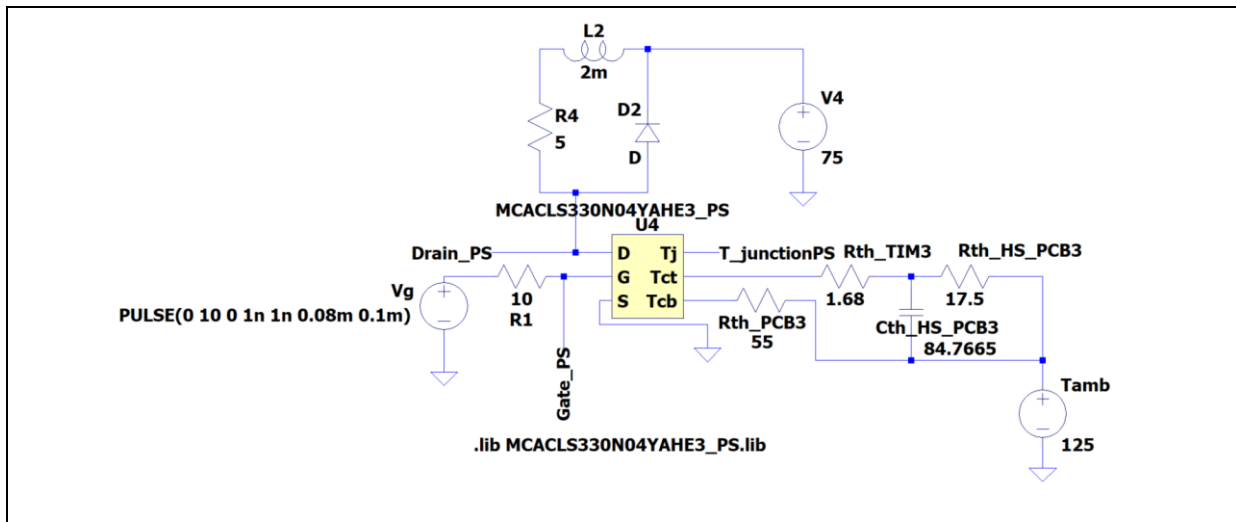


Figure 14: Low-side driver circuit for MCACLS330N04YAHE3 with inductive and resistive loads and an embedded thermal model

Following the electro-thermal analogy, this behavioral current source represents the power dissipated by the MOSFET and is calculated from the voltage between the Drain (D) and Source (S) terminals multiplied by the current flowing through the device. The V_d source shown in the first line of the Figure 13 netlist does not represent a physical component. Instead, it is used as a modeling technique to measure the current through the MOSFET and calculate instantaneous power.

$$i(v_{ds}, i_d) = (v_d - v_s)(i_d) \quad (\text{Eq. 11})$$

This approach provides a simple way to couple the electrical and thermal models. However, because the current through the V_d source can include current associated with parasitic capacitances, it may differ slightly from the MOSFET's actual conduction current. As a result, the calculated power may differ slightly from the actual device's power dissipation.

Figure 15 provides a clear comparison of the junction temperature obtained from the embedded Cauer model in Figure 11 and the results obtained using the schematic model in Figure 14, with the accurate MOSFET terminal power used as the input. The two results show close agreement under the simulated conditions.

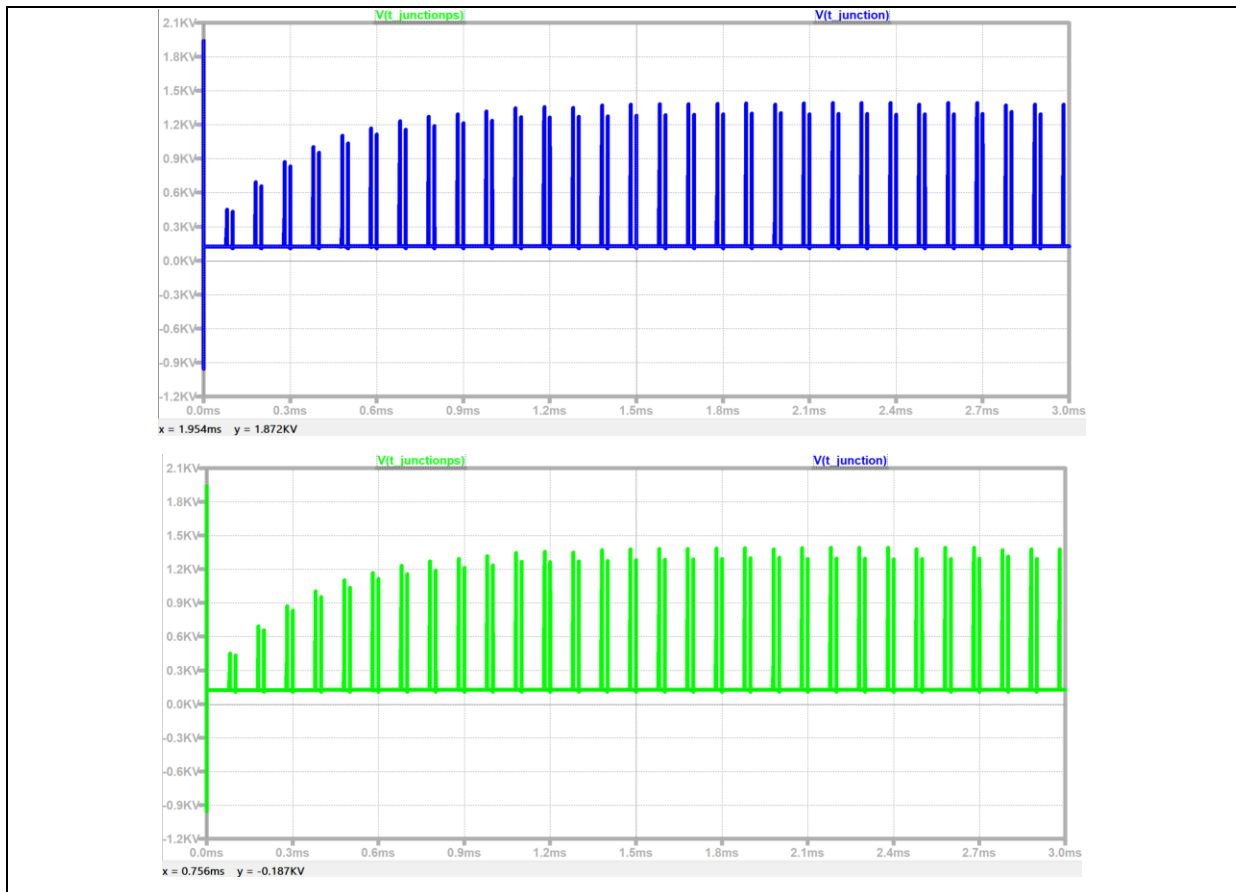


Figure 15: MCACLS330N04YAHE3 thermal response simulation. The upper waveform (blue) shows the junction temperature from the embedded thermal model, while the lower waveform (green) shows the result from the schematic thermal model

7. CONCLUSION

This application note described the thermal modeling approach used by MCC to simulate junction temperature under transient power pulses for devices with available transient thermal impedance characterization.

The theoretical basis, model extraction process, and SPICE simulation implementation were presented to provide a practical and transparent approach that designers can replicate in their own simulations.

For further information on thermal management and MCC's Dual-Side Cooling technology, explore the following resources:

- [Watch: Dual-Side Cooling MOSFETs: DSC vs. Traditional DFN5060 Comparison](#) — See how MCC's Dual-Side Cooling (DSC) MOSFET compares with a traditional DFN5060 package.
- [Thermal Management: A Guide to Greater MOSFET Performance and Cooling](#) — Learn the fundamentals of MOSFET thermal management and practical approaches to improving cooling performance.
- [Thermal Modeling and Heat Dissipation: Design for Reliability and Better Efficiency](#) — Explore MCC's additional information sharing on thermal modeling, heat dissipation, reliability, and efficiency.

As design trends and challenges evolve, MCC will remain your total solutions partner, delivering insights and innovative products to help you win.

Use the MCC website [chatbot](#) to contact us for support with heat dissipation, thermal modeling, or other challenges you may encounter when designing your products.

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